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Performance of Power Consumption Using Double-Tail Comparator

Gomathi M.R, Suresh. S

Abstract— The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented. From the analysis, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

Keywords- Dynamic comparator, ADC converter , Power consumption, Delay time

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs)[1]. Many high- speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [10]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller.

In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs [1].

Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges [2] [3]. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems.

Gomathi M.R, PG Student,M.E VLSI Design,
Suresh,S Assistant Professor

These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies [5].

II. COMPARATOR

A. Single Tail Comparator

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset and random decision errors and kick-back noise. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analysed, based on which the proposed comparator will be presented. Comparator having two operation modes, the reset phase and the evaluation phase. The modes of operation depend on the clock input given. Clk = 0 known as reset phase and clk = Vdd known as evaluation phase. When clk = 0, nMOS transistor is in off and pMOS transistor is in on. When clk = Vdd, nMOS is in on and pMOS transistor is in off.

B. Block Diagram description

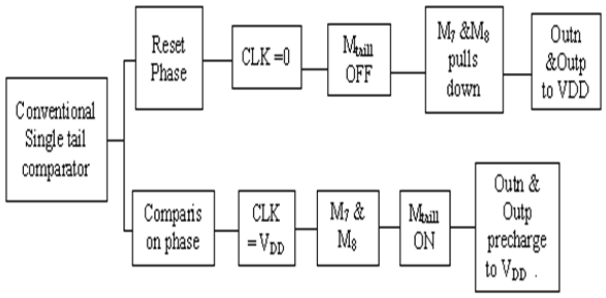

Fig. 1 Block Diagram of Single Tail Comparator

Comparator having two operation modes, the reset phase and the evaluation phase. The modes of operation depend on the clock input given. Clk = 0 known as reset phase and clk = Vdd known as evaluation phase. When clk = 0, nMOS transistor is in off and pMOS transistor is in on. When clk = Vdd, nMOS is in on and pMOS transistor is in off.

When clk = 0, the circuit is in reset phase, while Mtail is off. The reset transistors M7 and M8 became on. These reset transistors pull both output nodes Outn and Outp to Vdd.

In the evaluation phase, clk = Vdd, reset transistors M7 and M8 became off and Mtail is on [7]. Outn and Outp, which had been pre-charged to Vdd, start to discharge. Discharging rates are different depending on the corresponding input voltage INN and INP. Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence Output voltages, which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltages.

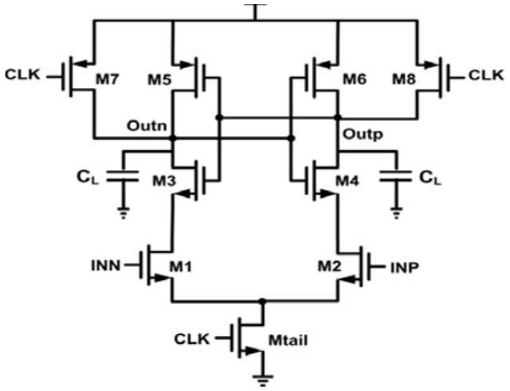

Fig.2 Schematic Diagram of Single Tail Comparator

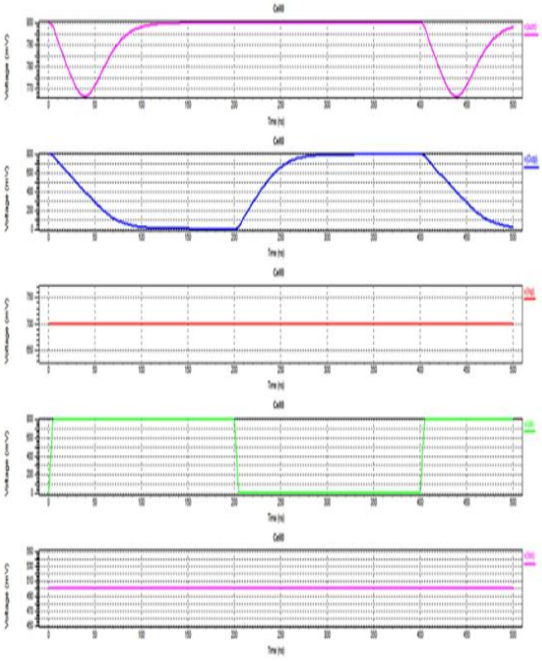

Fig.3 Output waveforms of Single Tail Comparator

C. Double Tail Comparator

Double tail architecture has two tail transistors .This comparator is used for low power applications. In this technique, increase the voltage difference between the output nodes in order to increase the latch regeneration speed.

For this purpose, two control transistors have been added to the first stage in parallel to M3 and M4 transistors but in a cross-coupled manner.

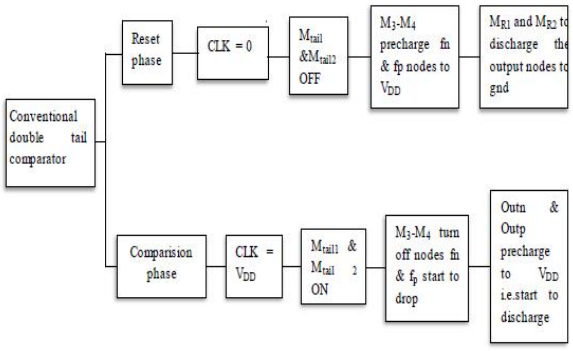

Fig. 4 Block Diagram of Double Tail Dynamic Comparator

D. Schematic Diagram description

Double tail comparator has two operation modes, the reset phase and the decision making phase. The modes of operation depend on the clock input given. Clk = 0 known as reset phase and clk = Vdd known as evaluation phase. When clk = 0, nMOS transistor is in off and pMOS transistor is in on. When clk = Vdd, nMOS is in on and pMOS transistor is in off[9].

The operation of the proposed comparator is as follows. When clk = 0, the reset phase, both the tail transistors Mtail1 and Mtail2 are in off to avoiding static power. Transistor M3 and M4 are in on. M3 and M4 pulls both fn and fp nodes to Vdd, hence transistor MC1 and MC2 are cut off. The circuit has two intermediate stage transistors MR1 and MR2. These transistors reset both latch outputs to ground**.**

During decision-making phase, clk = Vdd, both the tail transistors are on, M3 and M4 transistors are off. At the beginning of this phase, the control transistors MC1 and Mc2 are still off (since fn and fp are about Vdd). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1).

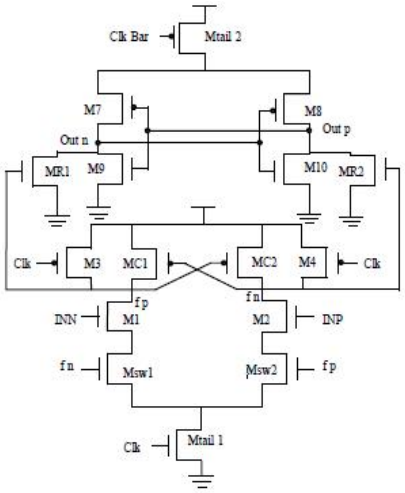

Fig.5 Schematic Diagram of Double Tail Dynamic Comparator

As long as fn continues falling, the corresponding pMOS control transistor (MC1 in this case) starts to turn on, pulling fp node back to the Vdd, so another control transistor remains

off, allowing fn to be discharged completely.Fig.7 represents the Transient simulation of double tail comparator.

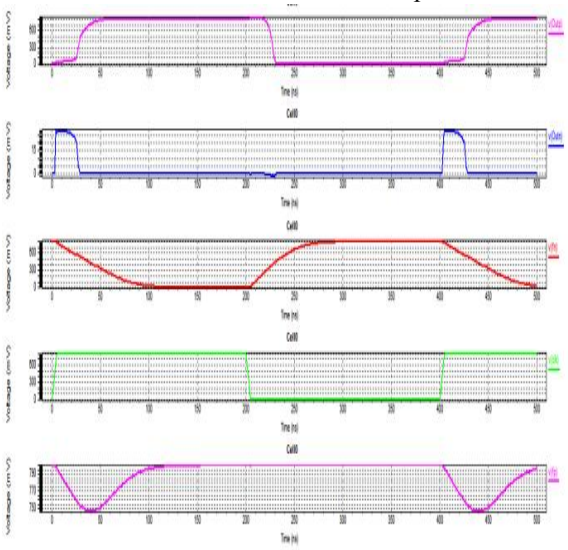

Fig.6 Output waveforms of Double Tail Comparator

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD. (during the reset phase)[11] [12], both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from *V*DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch [15].

E. Simulation Result:

Tanner EDA tools is used for analog and mixed-signal ICs and MEMS design offers designers a seamless, efficient path from design capture through verification. Application of Tanner tool is for Power Management, Life Sciences / Biomedical, Displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaic, Consumer Electronics and MEMS.

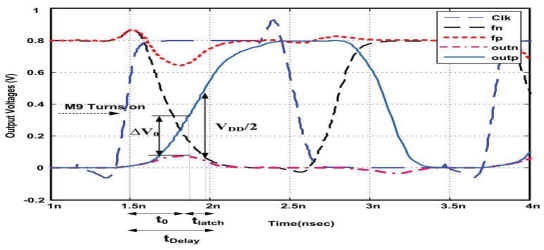

Fig .7 Transient simulation of conventional double tail dynamic comparator

Fig.8. Output of CLK, CLK, INN, INP, OUTN, OUTP

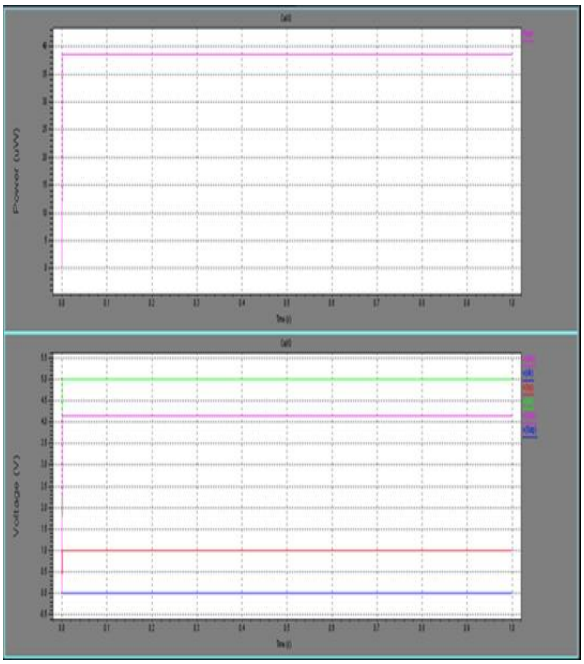

Fig .9. Output Power Graph

TABLE I
Performance Comparison

Comparator Structure	Conventional Dynamic Single Tail Comparator	Double Tail Comparator
Technology CMOS	180nm	90nm
Supply Voltage	0.8V	0.8V
Delay	25ps	14ps
Average Power	32.35µwatts	3.8µwatts
Time	20ns	66ns

III. CONCLUSION

In this paper we presented a delay analysis for conventional dynamic single tail and double tail comparator. We also analyzed with low voltage low power capability was proposed in order to improve the performance of the comparator. In proposed comparator the delay and energy per conversion is reduced to a greater extent in comparison with the conventional dynamic comparator and double tail comparator. In other words Execution time and power consumption is further reduced in the proposed comparator.

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