International Journal on Applications in Information and Communication Engineering
Volume 1: Issue 6: June 2015, pp 5-11. www.aetsjournal.com ISSN (Online) : 2394-6237

Low-Power Low-Voltage High-Speed Performance Improvement Analysis Of Double Tail Comparator

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Abstract— Comparator is one of the fundamental building blocks in most analog-to-digital converters (adcs). Many high speed adcs, such as flash adcs, require high-speed, low power comparators with small chip area. A dynamic regenerative comparator in a low-power 25-nm complementarymetal–oxide–semiconductor process is presented. Based on the analysis, a new dynamic comparatoris proposed, wherethe circuit of a conventional double tail comparator consisting oftwo cross-coupled inverters is modified for fast operation, low power evenwith a low supply voltage and small area. The advantagesof a high-impedance input, rail-to-rail output swing, robustnessagainst the influence of mismatch, and no static power consumptionare kept. A positivefeedback mechanism to regenerate the analog input signal into afull-scale digital level. Without complicating the designand by adding few transistors, the positive feedback duringthe regeneration is strengthened, which results in remarkablyreduced delay time. It is shown that inthe proposed dynamic comparator both the power consumptionand delay time are significantly reduced. Kickback noise is also reduced when the input voltage is not disturbed by large voltage variation.

Keywords: Comparator, analog-to-digital converters, Kickback noise, positivefeedback mechanism, double tail comparator etc.

I. INTRODUCTION

A. Basic Cmos Comparator

The schematic symbol and basic operation of a voltage comparator are shown in fig1.1. The comparator can be thought of as a decision making circuit. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic0.

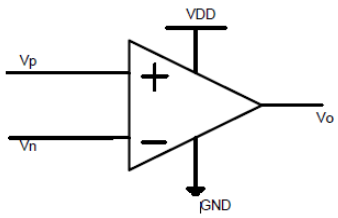

Fig.1 Schematic symbol

$V_P < V_N$ then V_O = VSS= logic 0.

$V_P > V_N$ then V_O = VDD= logic 1.

Comparator operation

An analog signal is one that can have any of a continuum of amplitude values at a given point in time .In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is imp0ortant for the comparator to pass quickly through the transition region. The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator 7 emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

B. CMOS Comparator Characterization

A positive voltage applied at the *Vp*input will cause the comparator output to go positive, whereas a positive voltage applied at the *VN* input will cause the comparator output to 10 go negative. The upper and lower voltage limits of the comparator Output are defined as *V OH* and *VOL* respectively.

Static Characteristics

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Fig.2. As shown in this figure. The output of the comparator is high (V*OH)* when the' difference between the no inverting and inverting inputs is positive, and low *(VOL)* when this difference is negative. Even though this type of behaviour is impossible in a real-world situation, it can be modelled with ideal circuit elements

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with mathematical descriptions. One such circuit model is comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the fig.3.

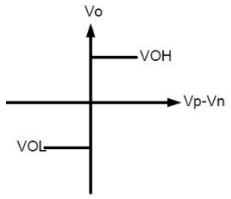

Fig.2 Ideal Transfer curve of a comparator

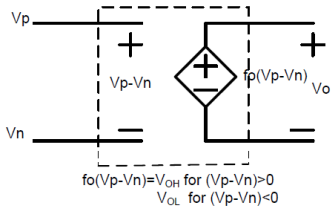

Fig.3 Model for an ideal comparator

The second no ideal effect seen in comparator circuits is input-offset voltage, *Vos*. In Fig.1 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value *+Vos,* then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit for a given design. Fig.4 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Fig.5 The ± sign of the offset voltage accounts for the fact that *Vos* is unknown in polarity.

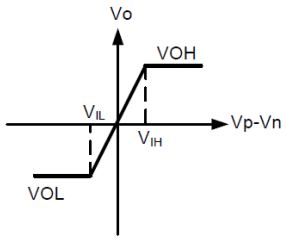

Fig.4 Transfer curve for a comparator with finite Gain

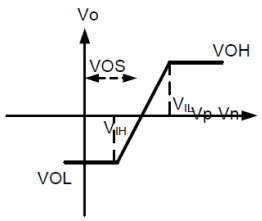

Fig.5 Transfer curve including input-offset voltage

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. In addition, there will also be an input common-mode resistance, *Ricm.* All these aspects can be modelled in the same manner as was done for the opamp. Because the input to the comparator is usually differential, the input common-mode range is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation.

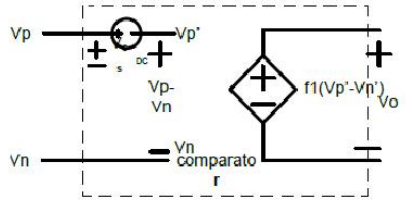

Fig.6 Model for a comparator including input-offset voltage

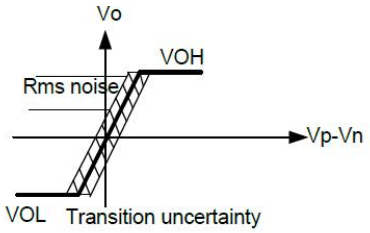

Fig.7 Influence of noise on a comparator

Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modelled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Fig.7. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.

Dynamic Characteristics

The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Note that there is a delay between the input excitation and the output response. This· time difference is called the propagationdelaytimeof the comparator. It is a very important parameter since it is often the speed limitation in the conversion rate of an *A/C*onverter. The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which further increases in the input voltage will no longer affect the delay .This mode of operation is called slewingor slewrate.

II. METHODOLOGY

A. Low Power Design

The density and speed of integrated-circuit computing elements have increased exponentially for several decades, following a trend described by Moore's Law. While it is generally accepted that this exponential improvement trend will end, it is unclear exactly how dense and fast integrated circuits will get by the time this point is reached. Working devices have been demonstrated which were fabricated with a MOS Transistor channel length of 6.3 nm using conventional semiconductor materials, and devices have been built that used carbon nanotubes as MOSFET gates, giving a channel length of approximately one nanometer. The density and computing power of integrated circuits are limited primarily by power-dissipation concerns. The overall power consumption of a new personal computer has been increasing at about 22% growth per year. This increase in consumption comes even though the energy consumed by a single CMOS logic gate to change state has fallen exponentially with the Moore's law shrinking of process feature size. An integrated-circuit chip contains many capacitive loads, formed both intentionally (as with gate-to-channel capacitance) and unintentionally (between conductors which are near each other but not electrically connected). Changing the state of the circuit causes a change in the voltage across these parasitic capacitances, which involves a change in the amount of stored energy. As the capacitive loads are charged and discharged through resistive devices, an amount of energy comparable to that stored in the capacitor is dissipated as heat:

$$E_{stroed} = \frac{1}{2} C V^2$$

The effect of heat dissipation on state change is to limit the amount of computation that may be performed on a given power budget. While device shrinkage can reduce some parasitic capacitances, the number of devices on an integrated-circuit chip has increased more than enough to compensate for reduced capacitance in each individual device. Some circuits – dynamic logic, for example – require a minimum clock rate in order to function properly, wasting "dynamic power" even when it has nothing to do. Other circuits – most famously, the RCA 1802, but also many later chips such as the WDC 65C02, the 80C85, the Free scale 68HC11 and some other CMOS chips – use "fully static logic" that has no minimum clock rate, but can "stop the clock" and hold their state indefinitely. When the clock is stopped such circuits use no dynamic power but they still have a small, static power consumption caused by leakage current. As circuits shrink, sub threshold leakage current becomes more important. This leakage current results in power consumption, even when no switching is taking place; with modern chips, this current is frequently more than 50% of power used by the IC.

B. Reducing Power Loss

Loss fromsubthreshold leakage can be reduced by raising the threshold voltage and lowering the supply voltage. Both these changes slow the circuit down significantly, and some modern low-power circuits use dual supply voltages to provide speed on critical parts of the circuit and lower power on non-critical paths. Some circuits even use different transistors (with different threshold voltages) in different parts of the circuit, in an attempt to further reduce power consumption without significant performance loss. Another method used to reduce static power consumption is power gating: the use of sleep transistors to disable entire blocks when not in use. Systems which are dormant for long periods of time and "wake up" to perform a periodic activity are often in an isolated location monitoring an activity. These systems are generally battery- or solar-powered; power consumption is a key design factor. By shutting down a functional but leaky block until it is used, leakage current can be reduced significantly. For some embedded systems that only function for short periods at a time, this can dramatically reduce power consumption.

Two other approaches exist to lowering the power cost of state changes. One is to reduce the operating voltage of the circuit, as in a dual-voltage CPU, or to reduce the voltage change involved in a state change (making a state change only, changing node voltage by a fraction of the supply voltage low voltage differential signaling, for example). This approach is limited by thermal noise within the circuit. There is a characteristic voltage (proportional to the device temperature and to the Boltzmann constant), which the state switching voltage must exceed in order for the circuit to be resistant to noise. This is typically on the order of 50–100 mV, for devices rated to 100 degrees Celsius external temperature (about 4 kT, where T is the device's internal temperature in kelvins and k is the Boltzmann constant).

The second approach is to attempt to provide charge to the capacitive loads through paths that are not primarily resistive. This is the principle behind adiabatic circuits. The charge is supplied either from a variable-voltage inductive power supply, or by other elements in a reversible-logic circuit. In both cases, the charge transfer must be primarily regulated by the non-resistive load. As a practical rule of thumb, this means the change

rate of a signal must be slower than that dictated by the RC time constant of the circuit being driven. In other words, the price of reduced power consumption per unit computation is a reduced absolute speed of computation. In practice although adiabatic circuits have been built, they have been difficult to use to reduce computation power substantially in practical circuits. Finally, there are several techniques used to reduce the number of state changes associated with a given computation. For clocked- logic circuits the technique of clock gating is used, to avoid changing the state of functional blocks that are not required for a given operation. As a more-extreme alternative, the asynchronous logic approach implements circuits in such a way that a specific externally supplied clock is not required. While both of these techniques are used to varying extents in integrated circuit design, the limit of practical applicability for each appears to have been reached.

C. Conventional Comparator

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise offset and random decision errors, and kick-back noise. A comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analysed, based on which the proposed comparator will be presented.

D. Conventional Dynamic Comparator

The conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption. The advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time.

E. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

- The voltage difference at the first stage outputs (Vfn/fp) at time t0 has a profound effect on latch initial differential output voltage (V0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.
- Comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. EXISTING METHOD

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Out$n$ and Out$p$ to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8are off, and Mtail is on. Output voltages (Out$p$, Out$n$), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage(INN/INP).VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5and M4, M6).

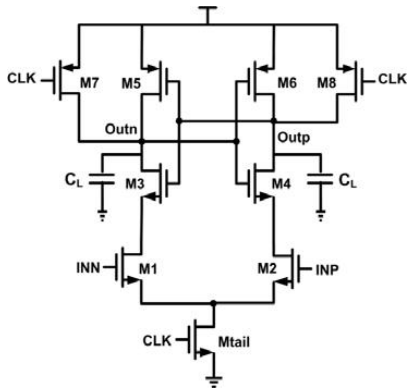

Fig.8 Conventional Dynamic Comparator

Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. The delay of this comparator is comprised of two time delays, t0 and tlatch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. The second term, tlatch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of _Vout= VDD/2 has to be obtained from an initial output voltage difference _V0 at the falling output (e.g., Outp).The total delay is given by

tdelay= t0+tlatch

The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input difference voltage (_Vin). By reducing Vcm, the delay t0 of the first sensing phase increases because lower Vcm causes smaller bias current (Itail). On the other hand a delayed discharge with smaller Itail results in an increased initial voltage difference (_V0), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing of t0 and reducing of tlatch will finally lead to an increase in the total delay. The advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. Another important drawback of this structure is that there is only one current path, via tail transistor *M*tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters).

B. Conventional Double Tail Comparator

This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset. The operation of this comparator is as follows , During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3- M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK =VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes _Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

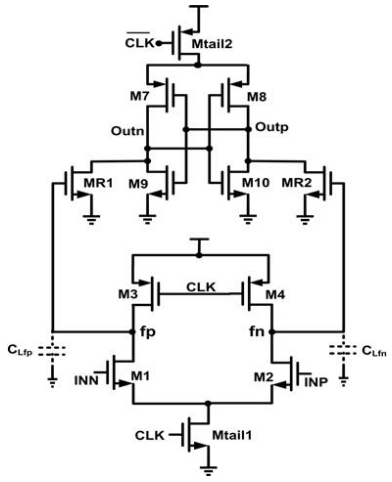

Fig.9 Conventional Double tail Comparator

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called "kickback noise." Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts. The voltage difference at the first stage outputs (_Vfn/fp) at time t0 has a profound effect on latch initial differential output voltage (_V0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator. In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective trans conductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption.

C. Proposed Conventional Double Tail Comparator

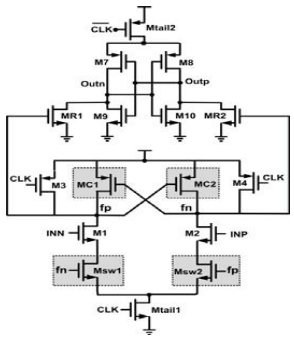

Fig.10 Proposed Conventional Double tail Comparator

The main idea of the comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 andMc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner. The operation of the proposed comparator is as follows, During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1).Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on, a current

from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [*M*sw1 and *M*sw2].

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

D.Delay Analysis:

The dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (_V0) at the beginning of the regeneration (t = t0); and second, it enhances the effective transconductace (gmeff) of the latch. Each of these factors will be discussed in detail.

(i) Effect of Enhancing_V0:

As discussed before, we definet0, as a time after which latch regeneration starts. In other words, t0 is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence.

(ii) Effect of Enhancing Latch Effective Transconductance:

As mentioned before, in conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. In our comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the VDD at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened. By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes advantage of an inner positive feedback in double-tail operation, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of VTh/VDD, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator.

(iii)Reducing the Energy Per Comparison:

It is not only the delay parameter which is improved in the modified comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. While double tail structure takes advantage of input-output isolation and thus the minimum kickback noise, the conventional dynamic comparator and our proposed structure has nearly similar kickback noise. However, in our proposed comparator since control transistors are not supposed to be as strong as the latch transistors in conventional dynamic comparator, it is possible to determine the size of those transistors in a way that keeps the advantages of the speed enhancement and power reduction, while reducing kickback noise. Besides, for some applications where kickback becomes important, it is possible to apply simple kickback reduction techniques, such as neutralization to remarkably reduce the kickback noise.

IV. MODIFICATION

A. Modification Of Proposed Double Tail Comparator

The modified comparator .it is designed based on the proposed comparator. Compared with proposed it provides, better performance of double tail comparator in low voltage applications. Drawback of proposed comparator is, the nodes fn and fp starts to drop with different rates according to the input voltages. The continues falling of fn, the corresponding transistor MC1 starts to turn on and fp node backs to VDD. Node fn to be discharged completely (MC2 off).When one of the control transistors (MC1) turns ON, a current from VDD is drawn to the ground via input and tail transistor. Resulting a static power consumption. For this purpose two switching transistors (Msw3 and Msw4) have been added to Msw1 and Msw2 in series manner. Modified comparator reduced the delay and power.

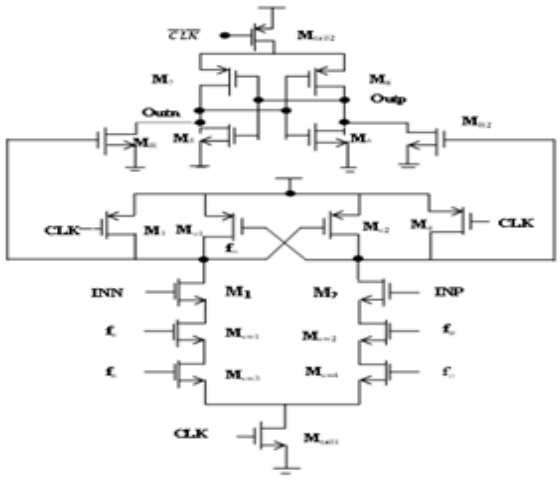

Fig.11 Circuit for Modified Proposed Double tail Comparator

Design Considerations

The size of transistors can be determined by the time it takes that one of the control transistors turns on must be smaller thant0 transistor(regeneration time).It can be achieved by designing first and second stage of tail currents. Low threshold PMOS devices can be used as control transistors leading to faster turn on in the fabrication technology. Another consideration is effect of mismatch between the controlling transistors of the comparator. Mismatch is a spatial noise spread. In this modification mismatch effect is reduced. The large voltage variations in the internal nodes are coupled to the input disturbing the input voltage called ―kick back noise. Most efficient comparators generate this type of noise. The minimum kickback noise in the double tail comparator.

V. Conclusion and Future Work

A new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. The delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. A positivefeedback mechanism to regenerate the analog input signal into afull-scale digital level.Without complicating the designand by adding few transistors, the positive feedback duringthe regeneration will be strengthened, the delay time will be reduced in future work. It will be show inthe proposed dynamic comparator both the power consumptionand delay time will be reduced and also Kickback noise will be reduced

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