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IMPLEMENTATION OF LPT USING SPIDER TECHNIQUE

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Abstract— A LP broad side test set is designed from a functional broadside set with the derivation of skewed-load test cubes in Built in Self Test circuits. In order to cope up with the functional operation criteria, our work concentrates on the percentage of values indefinite values in the tests performed. The double effect of programmable truncated multiplication and fault tolerant Digital Signal processing (DSP) design is put on to reduce voltage beyond critical timing level. Timing modulations properties of truncated multiplication are are examined for the betterment of fault tolerant designs, reducing error correction burdens, and extending the system operating voltage range. The lower power test schemes along with Razor technique is implemented with the original DSP. Only drawback is the degradation of the output signal-to-noise ratio.

Keywords **--** Signal processing, BIST, Advanced Razor technique.

I. INTRODUCTION

In VLSI circuits, voltage scaling is implemented to decrease dynamic power consumption and to achieve static power management. If chosen scaling factor is K, then the factor of reduction in power consumption is obtained as K^2 [1]. The progress in CMOS technology exploits scaling to avoid issues from process voltage temperature (PVT) deviations.

In digital signal processing (DSP), voltage over scaling (VOS) levels is incorporated for energy consumption in retaining DSP function. The main features offered in contrast to timing constraints are presentation of appraisal of subsystem that delivers estimation in case of fault detection and skills that vary the data capture by supplementing the latches or flip flops on the critical path by extending execution time[2-4]. These combined features promises low power systems with moderate functionalities with a compromise on signal degradation and execution time.

Power conservation obtained under fault tolerant techniques are decided by PVT variations, circuit design and data input. Conservation is further improved with the aid of statistical timing distribution that shows the estimation of percentage of samples. Truncated multipliers are incorporated for power consumption, area and yields to various timing distributions. The combined performance of VOS and truncated multiplication is exploited by the custom-designed fixed point multiply and accumulate (MAC) structure[3]. Power consumption seems to be more for scan-based test and this issue is compensated by using functional broadside tests. Hence the switching activity is minimized.

II. TEST PATTERN APPLICATION

The function of clock in a scan structure is scanning in and out of the test pattern and its application. One clock cycle is enough for a full scan of the test pattern application. Whereas in partial scan, the sequential logic left in the CUT is clocked frequently.

a) Test-per-scan

The generated test pattern is fed to the CUT input in a synchronous circuit. The test pattern is shifted to the scan chain and clocking is triggered. Then the CUT output pattern is latched and terminated to the scan chain for further processing.parallel scanning of previous and next test pattern demands*n* clock cycles for an *n*-stage scan path, which extends the duration of the test pattern processing by the CUT. Hence the duration of this test-per-scan strategy (Fig. 4) is more:

III. RAZOR IMPLEMENTATION

The programmable truncated multiply and-accumulate (PTMAC) architecture is structured as a means to apply PTM in low-power biomedical applications with a need for modest DSP, such as ECG filtering or fall detection [10]. In our work, it is exploited as a platform to entertain and for grouping of programmable truncation and fault tolerance.

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The Testing Based Low Power with PTMAC is introduced as an outspread of BISTY to support general DSP architecture. LT-PTMAC is inexpensive towards implementing PTM with low power applications[5].

The total control unit functions under five stage program, memory blocks and pipeline in a multi-bus Harvard configuration. The other units are I/O connectivity interfaces, an arithmetic unit designed with MAC structure of 16-bit PTM, a 40 bit accumulator for scaling and rotating the accumulated value. The same is explained in the upcoming sections, in order to achieve a flexible unit that trades energy for signal and performance degradation[1].

The accumulator unit of the LT-PTMAC has to deal with the fault tolerance, and it is obtained by introducing a fault tolerant version named Razor Accumulator. The original flip-flops were substituted by a version of the Razor registers which is newly implemented[6-9].

The projected amplified cells are structured and accumulated as library cells for post synthesis insertion. These cells responds to the unique implementation that is Razor implementation, where the Razor registers containing the shadow latch is replaced with shadow-flip-flop. Hence it avoids combination issues. The meta-stability sensor required in Razor implementations is programmed as the delay of an inverter, which acts as a limitation to the hold time of the Razor accumulator[4].

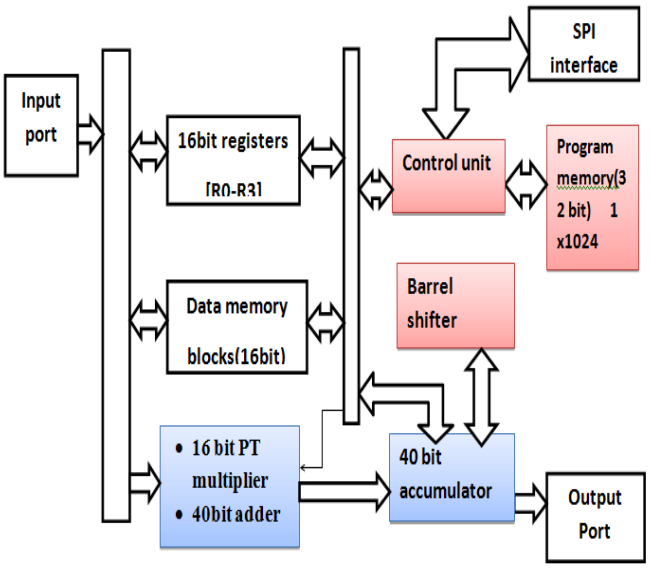

Fig.1. CUT for LT-PTMAC top level diagram

The architecture has to be modified in a Razor implementation for error rectification by allocating a special clock cycle for the data error. The error is to be rectified by replacing with the correct data. From different possible pipeline management plans recommended in the Razor works, architectural repetition was suggested the most suitable for PTMAC. All the implementations perform write / read or arithmetic operations.

So a simple repeat strategy where a stall flag is issued in the presence of Razor errors, which easily corrects faulty results with a small area overhead, when avoiding issues with post incrementing address pointers. The instruction of an execution cycle on the sleep mode Low Power Razor-augmented PTMAC (SL RPTMAC) can thus be divided in four possible stages.

The proposed DSP includes a control unit operating in a five-stage pipeline, program and memory blocks in a multi-bus Harvard configuration, some I/O connectivity and an arithmetic unit consisting of a MAC structure with a 16-bit PTM, a 40-bit accumulator, and a 40-bit barrel shifter for scaling and rotating the accumulated value.

Two classes of efficient simulation-based procedures exist for the generation of functional broadside tests. The procedure usedin this brief extracts functional broadside tests from functional test sequences. When the functional test sequences satisfy functional constraints on primary input sequences, the functional broadside tests that are extracted from them satisfy the same constraints. For the discussion in this brief, the primary input sequences are assumed to be unconstrained. Functional test sequences are generated by a low complexity sequential test generation process that does not consider target faults.

This is important since it implies that the test cubes preserve many of the values that are assigned by functional broadside tests. The test cubes thus create functional operation conditions throughout the circuit. The execution cycle of an instruction on the Razor-augmented PTMAC (RPTMAC) can be thus divided in four possible stages.

a) EP:

The initial half clock cycle is the execution phase where the instruction starts its execution, but because of hold time requirements it does not reach any of the augmented registers.

b) AP:

The second half clock cycle is the arrival phase (AP) where the instructionfinishes its execution and data is allowed toreach the destination registers. Instructions that fail to do will generate either an Error or a System Failure.

c) EDP:

The third half clock cycle is the error detection phase, where signals that failed completion .can finish their executioncausing a Razor error. Instructions failing to finish during the third stage will cause a System Failure, limiting the minimumsupply voltage applicable to the system.

d)ECP:

The fourth stage is the error correction phase (ECP).In the event of an Error being flagged in EDP, a multiplexerwill feed the output of the value previously captured by theShadow Latch into the input of the Main Flip-flop, and theerror signal will be cleared.EP and AP stages represent a regular execution stage of a pipeline,while the last two stages (EDP and ECP) overlap with the executionstage of the next instruction in Fig. 7. Detecting an error in the EDPphase causes either the ECP of the faulty instruction or the AP phaseof the following one to update the output of the Razor registers.

IV. RESULT AND DISCUSSION

This result is based on applying the BIST technique in the previously discussed chapter i.e., Razor based PTMAC technique. Now we are reducing the area , power and speed in this technique. The result for PTMAC, I-PTMAC and LT-PTMAC is shown in Table1 and Bar charts are given below.

Table 1 Comparison Results of Various PTMAC Architecture

PTMAC	**I-PTMAC**	**LT-PTMAC**
AREA		
Number of slice registers =228	Number of slice registers= 119	Number of slice registers= 96
Number of Slice LUTs= 534	Number of Slice LUTs = 421	Number of slice LUTs = 86
HDL Synthesis Report		
Adder/subtractors = 24	Adder/subtractors = 22	Adder/ subtractors = 15
Registers= 36	Registers = 18	Registers = 11
Latches =29	Latches = 22	Latches = 11
Comparators=8	Comparators = 6	Comparators=3
Multiplexers = 120	Multiplexers = 110	Multiplexers = 87
Tristates = 1	Tristates = 0	Tristates = 0
Xors = 145	Xors =122	Xors =89
Advanced HDL synthesis Report		
Adder/subtractors = 1	Adder/subtractors = 1	Adder /subtractors = 1
Counters = 2	Counters = 1	Counter =1
Registers = 198	Registers = 145	Registers= 34
Comparators = 1	Comparators = 2	Comparators = 1
Multiplexers = 89	Multiplexers = 73	Multiplexers = 43
Xors = 73	Xors = 73	Xors = 0
Power		
Logic = 0.926	Logic = 0.848	Logic = 0.712
IOs = 84.6816	IOs = 84.6816	IOs = 65.4896
Speed		
Minimum period = 2.432 ns	Minimum period = 2.101ns	Minimum period = 1.140 ns
Minimum input arrival time before clock = 1.912 ns	Minimum input arrival time before clock = 1.499 ns	Minimum input arrival time before clock = 1.302 ns
Maximum output required time after clock = 3.408 ns	Maximum output required time after clock = 3.408 ns	Maximum output required time after clock = 0.822ns
Maximum combinational path delay = 3.003 ns	Maximum combinational path delay = 3.003 ns	Maximum combinational path delay = 0.145ns
Total Real time to Xst completion = 18.38 secs	Total Real time to Xst completion = 17.42 secs	Total Real time to Xst completion = 8.02 secs
Total CPU time to XST completion = 19.06 secs	Total CPU time to XST completion = 13.24secs	Total CPU time to XST completion = 8.13 secs

From the experimental analysis, we got results on area, no of circuits, power, energy, time and speed for the three architectures. The results are compared and depicted as a bar chart as follow.

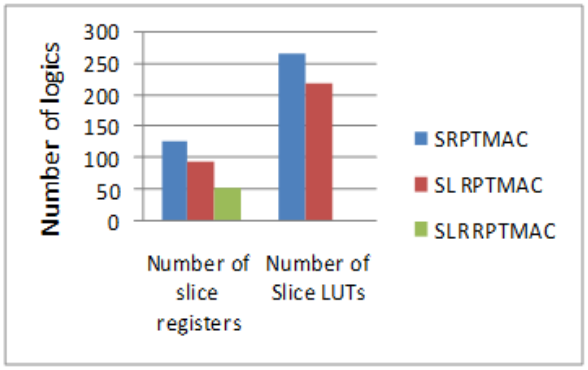

Fig.3. Area of slice registers analysis

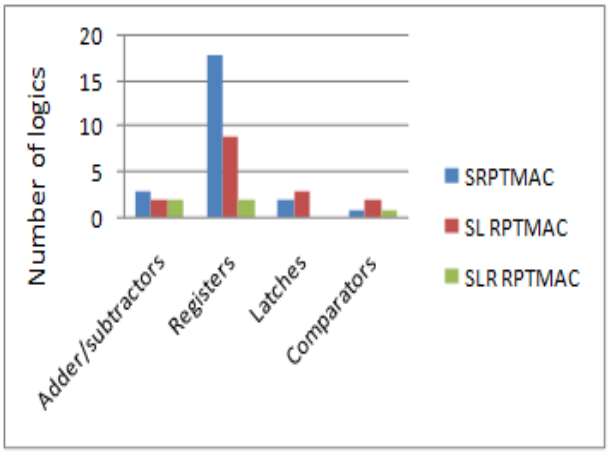

Fig. 4 .Adder/subtraction Multiplier and register analysis

PTMAC requires large area for slice registers and slice LUTs. On the other hand, LR-PTMAC requires small area. Also the area for slice registers is more than that for slice LUTs in PTMAC and I-PTMAC. But in LT-PTMAC number of slice LUTs is more than number of slice registers.

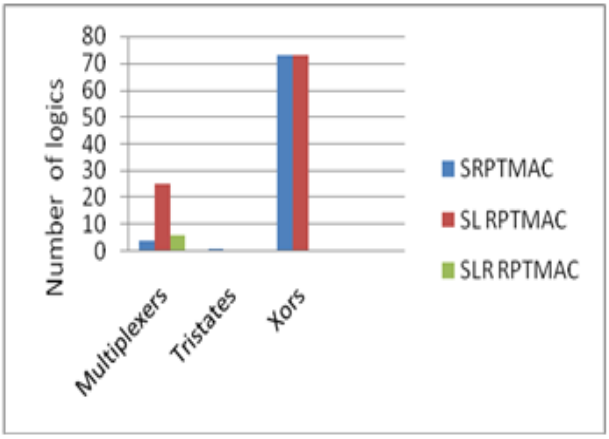

Fig. 5 Multiplexer and Tristates analysis

No. of adders, registers required for PTMAC is more than that required for others. I-PTMAC don't have latches while LT-PTMAC has more latches than PTMAC. Unlike PTMAC and I-PTMAC, LT-PTMAC has more comparators. It is also seen that in alls the three architectures, no of registers used is greater than no of adders, latches, comparators used. Among these three, PTMAC needs more multiplexers. There are no tri-states in I-RPTMAC and LT-PTMAC. Same number of XORs is used in PTMAC and PTMAC. LT-PTMAC doesn't have XORs in its architecture.

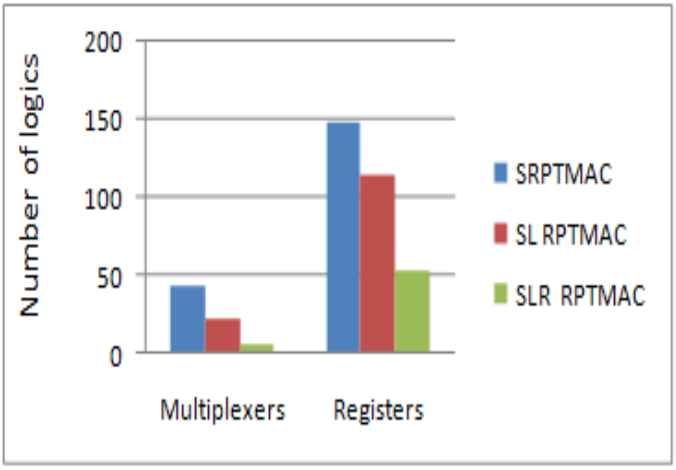

Fig. 6 Multiplexer and register analysis

By comparing the required no of multiplexers and registers, it is clear that in all the three architectures the no. of registers is more than the no. of multiplexers used.

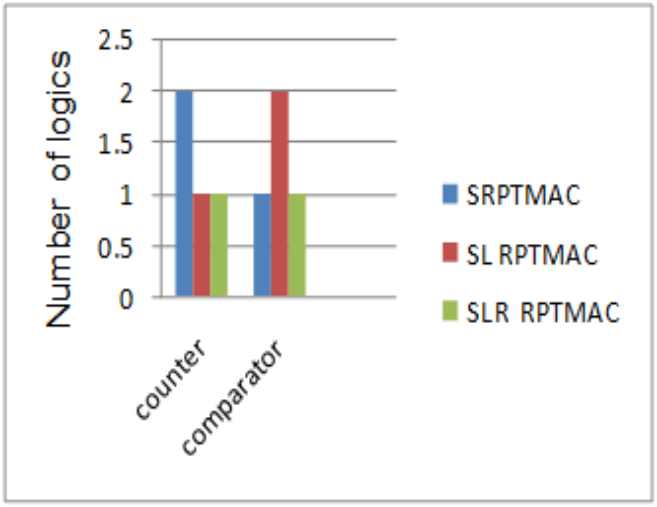

Fig. 7 Counter and comparator analysis

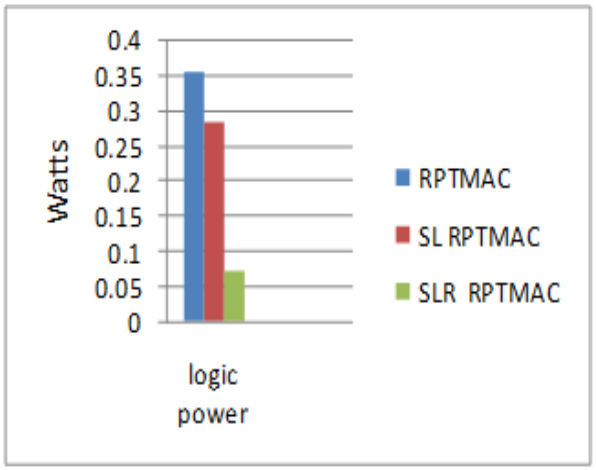

Fig.8 Power analysis of Logic power

From counter and comparator analysis, it is shown that in PTMAC and I-PTMAC the no. of comparators are less than counters. But in I-PTMAC more comparators are used than counters. Thus it is clear that the no of circuits required is less in LT-PTMAC (except counters).

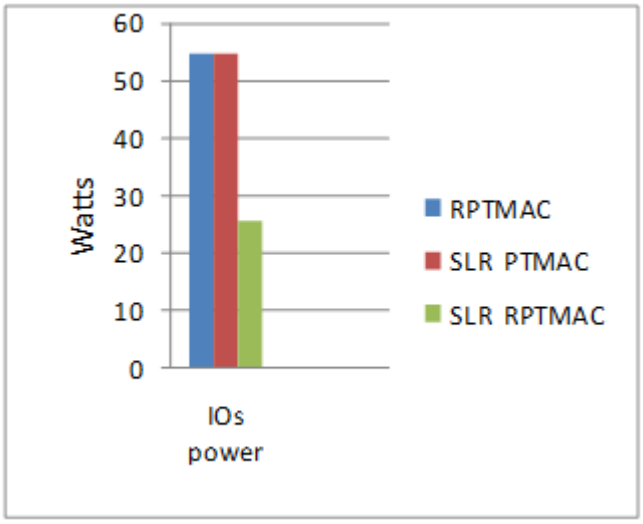

Fig. 9 Power analysis of IOs

Considering the logic power, the high value corresponds to PTMAC and low value corresponds to LT-

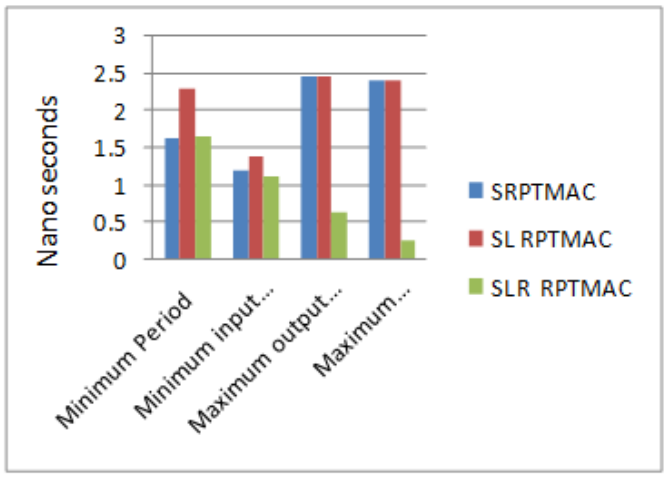

Fig. 10 Delay analysis

Equal IOs power is used by PTMAC and I-PTMAC. For LT-PTMAC IOs power is low. Among the three architectures LT-PTMAC has low logic power and low IOs power.

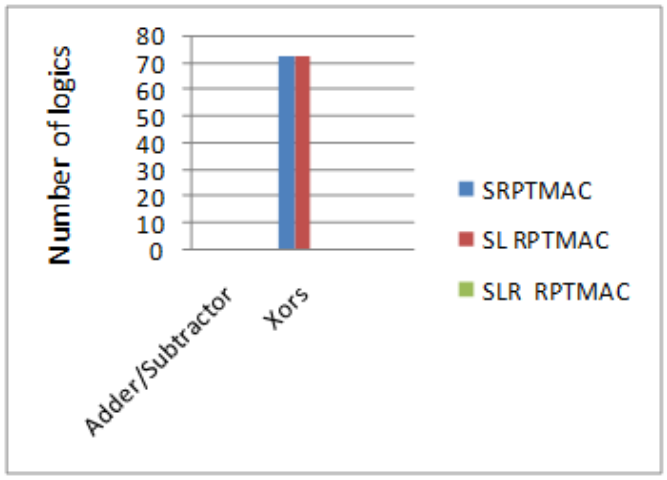

Fig.11 Adder/subtractor analysis

More number of XORs is used than multiplexers in PTMAC and I-PTMAC. Though there are no XORs in LT-PTMAC, it has few multiplexers.

V. CONCLUSION

The use of Advanced Razor based processor on a PT-MAC structure has been tested at a post synthesis simulation level to study the effect and interactions of both energy reducing techniques on a previously tested DSP design. The timing and power effects of VOS with error correction and the application of programmable truncated multiplication resulted in significant power reductions.It describes a test generation procedure brieflythat produces a compact low-power skewed-load test set by merging of skewed-loadtest cubes that are

derived from functional broadside tests. Such test cubes create functional operation conditions in sub circuits around the sites of detected faults. These conditions are preserved when a test cube is merged with other test cubes. For testable circuits, it is possible to use lower values in order to benefit from higher levels of test compaction. Test cube merging was implemented in a way that would ensure that the fault coverage of the final test set will not be limited by the fault coverage of functional broadside tests.

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