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Implementation of Low Power Hybrid Full Adder Design in GDI Technology

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Abstract— Hybrid logic style is widely used to implement full adder (FA) circuits. Performance of hybrid FA in terms of delay, power, and driving capability is largely dependent on the performance of XOR–XNOR circuit. In this article, a high- speed, low-power 10-T XOR–XNOR circuit is proposed, which provides full swing outputs simultaneously with improved delay performance. The performance of the proposed circuit is measured by simulating it in cadence virtuoso environment using 90-nmCMOS technology. The proposed circuit reduces the power delay product (PDP) at least by 7.5% than that of the available XOR–XNOR modules. Four different designs of FAs are also proposed in this article utilizing the proposed XOR–XNOR circuit and available sum and carry modules. The proposed FAs provide 2%–28.13% improvement in terms of PDP than that of other architectures. To measure the driving capabilities, the proposed FAs are embedded in 2-, 4-, and 8-bit cascaded full adder (CFA) structures. Results show that two of the proposed FAs provide the best performance for a higher number of bits among all theFAs. The proposed XOR–XNOR module is implemented with ten transistors, and it has a symmetrical structure which makes the layout of the proposed XOR–XNOR circuit less complex.

Keywords: lowpower, Hybrid Cmos Technolgy, Fulladder design

I. INTRODUCTION

In today's era, there are two main issues which we as a VLSI design engineers are facing todays i.e. Power Dissipation and Propagation Delay. We can work and design our circuit by using various technologies but on every design technologies there are some constraints which cannot be neglected. For that we can improve these two parameters to get the appropriate result. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. the addition of 1-bit binary numbers i.e. C A B as an input and two 1-bit binary numbers i.e. SUM and CARRY as an output. The full adder expression is mentioned below:-

$$SUM = A\ XOR\ B\ XOR\ C$$

$$CARRY = AB + BC + CA$$

1) Circuit Diagram:

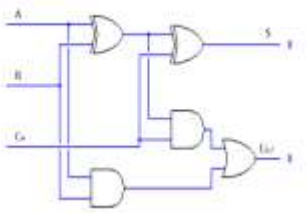


Figure 1. Full Adder

2)Full Adder using Half Adder:

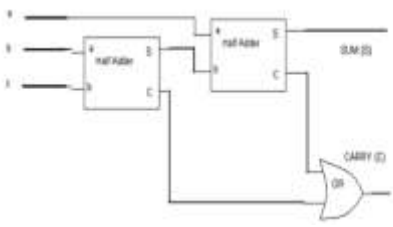


Figure 2 Full Adder using Half Adder

An N-bit adder can be constructed by cascading N-full adder circuits which is connected in seriesas shown in Figure.1.3

In the ripple carry adder, the carry bit 'ripples' from one stage to the other. For some input signals, no rippling effects occurs at all, while for others, the carry has to ripple from LSB to MSB. The expression of the ripple carry adder is:- For division, multiplication as well as exponential operations, full adder is one of the basic block. Where, "Tcarry" and "Tsum" equals to the propagation delays. Carry by-pass adder is also known as the carry skip adder. Carry skip adder has the four NAND Gate as an input for propagation signals in the 4-bit group. In carry skip adder, carry is generated along with the critical path from bit-1

and after propagating it through the remainder of the adder. Through the next 3 bits, the carry must ripple but after it skips the next four bit. Carry skip adder is quiet alike to the carry look-ahead adder. It is used to measure the group propagate signals and group generating signals to neglect the delay for the ripples if the group first generates a carry. The carry look-ahead circuit diagram is given below. The basic GDI cell was recommended by Morgenshtein. In the digital combinational circuit, this technique is utilize for the low power consumption.

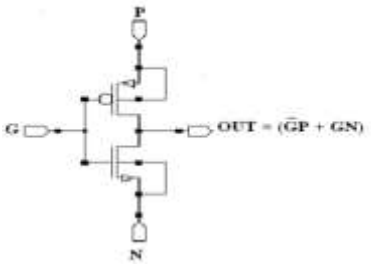


Figure 3 Basic cell of GDI

As compared to conventional complementary pass transistor logic, the Gate Diffusion Input technique is used to implement for increasing the spped and consumption of power in the circuit by using the logic operations.Gate Diffusion Input logic based on the various input values. In the Complementary Metal Oxide Semiconductor and the Gate Diffusion Technique, the prime difference is that in the Gate Diffusion Input Technique the Voltage drain-to drain source is not attached with the PMOS as well as the Ground is not attached to the NMOS which makes the Gate Diffusion Input circuit flexible.

II. RELATED WORKS

In this paper 8T full adder is used as a building block for 8-bit SQRT CSLA. 8T full adder is designed by XNOR hybrid CMOS design. To perform fast arithmetic operations, carry select adder is one of the fastest adders which is used for the processing of data complex.. The SQRT CSLA consists of 8T XNOR full adder. To achieve low power consumption 8T FA is used as the building block for ripple carry adder. A hybrid CMOS full adder with 8T is constructed by using 3T XNOR circuit. Since XNOR consists of 3 transistors only. The 3T XNOR circuit[1].In this paper, an architecture of 2:1 Multiplexer has been proposed In terms of delay, consumption of power and load capacitance of output the modified multiplexer of DCVSL 2:1 gives the better result. [2]. In this paper 1 bit full adder hybrid circuit has been proposed which consist of two techniques i.e. Pass transistor Logic and Gate Diffusion Technique. A single bit full adder cell is designed to represent the efficiency of the proposed architecture. For the designing of low power the method (GDI and PTL) is used. The typical complication in PTL and GDI technique is that the swing output is less because the Vdc is not included in the Gate Diffusion Input as well as the Pass transistor Logic. In conclusion of Power dissipation and delay it analyzed that the performed data of adder of hybrid is varies in between the PTL and the GDI. [3]In this paper, a new procedure is for diminishing the power absorption and developing the speed beyond reacting the noise margin is reviewed. In this paper, a technique of threshold voltage of the keeper transistor is diverse utilizing body bias generator circuit**[4].** This paper shows the correlative study of full adder utilizing various adiabatic logic architecture. Power analysis is executed at 45nm for various frequencies and output represents that at less frequencies Efficient Charge Recovery Logic (ECRL) absorbs 69% minimum power as compared it with the conventional CMOS logic design whereas at higher frequencies the power consumption of Secured-Quasi Adiabatic logic possess 71.8% lesser as compare it with the CMOS. SQAL is the advancement over ECRL[5]**.** This paper recommends Modified Positive Feedback Adiabatic Logic (MPFAL) which is utilize for ultra-low-power circuits. MPFAL is depend upon positive DC voltage ranging from 0.1V-0.3V. Half Adder and 1-bit full adder consolidate this technique used for the low power circuits[6]**.**In this paper, hybrid logic architecture utilize to construct the full adder. The circuit was appliance using Micro-wind tool in 90nm as well as 180nm Technology.. Delay in the signal propagation is calculated as 0.011ns and 0.087ns for 90nm and 180nm technology. Thus absorbing extremely low power and depend upon minimum time in comparison to the existing architecture for the double testing status[7]. The Adiabatic logic has become a solution of the

question of power dissipation. The proposed technique represents the minimization of power dissipation in comparison with the conventional CMOS architecture style switching events. We concluded that the power dissipation in PFAL is less as compare with the conventional CMOS logic circuits. Although PFAL go through the great switching period, therefore it is not suitable when the delay is critical. The Ripple Carry adder circuit is implemented with the help of these adder blocks and the carry adder is of 4-bits. The process of simulation is completed in the Tanner EDA environment..[9].

III. METHODOLOGY

A. Full Adder Design Approach

The design of the existing FA is divided into four major modules: two modules for carry generation and the other two for sum.

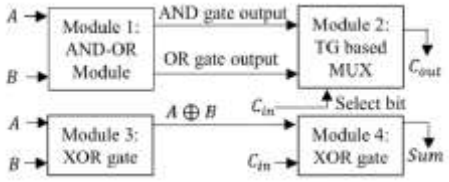


Figure 4. Block diagram of existing full adder.

1)Carry Generation

Therefore, the proposed carry generation part consists of a novel AND-OR module (module 1) based on TG and CPL logic. Within the AND-OR module, implementation of AND and OR gates are quite similar, except the fact that nMOS and pMOS transistors are interchanged.

The first condition for AND gate design in (1) is carried outby the pass transistor N2 and TG1, respectively. The later condition (2) is carried out by TG1. Here, conditions (3) and (4) are carried out by pass transistor P2 and TG2, respectively.

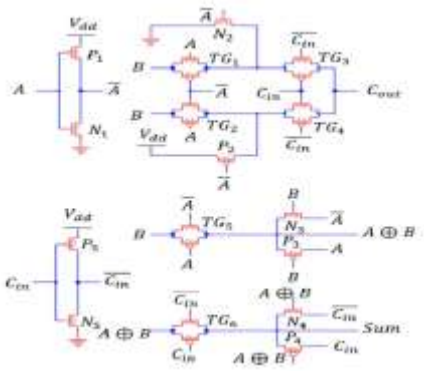


Figure 5. Schematic of the existing FA.

2)Sum Generation

The sum output of the proposed FA is generated by cascading two XOR modules (module 3 and 4). The XOR gates have exactly the same structure and are implemented using TGs and PTs. The circuit is simulated by randomly changing transistor width within the range of minimum to maximum allowable size. If a particle's current PDP < best PDP value so far found by that particle, then the current PDP is set as the particle's best PDP. In this way, after completing the desired number of iterations, the team's best value of PDP is chosen as the optimal PDP and the corresponding transistor widths are chosen for circuit implementation.

3)Performance of FA cells for various supply voltage

The post-layout simulation results on delay, power and Power Delay Product (PDP) for the supply voltage 0.4 V (minimum voltage in order to avoid sub-threshold operation),0.8 V (mid-point voltage between 0.4 V and 1.2 V) and 1.2 V (normal operating voltage) are represented using Fig. 3 and Table I.

4) Performance of FAs operating in cascade

To inspect scalability, FAs are extended into 4, 8, 16, 32and 64 bits in Ripple Carry Adder style as depicted in Fig. 3.4No intermediate buffer has been added while cascading FAs. However, they can be only extended to maximum 8-bits. This limitation happens due to the decline of signal strength(voltage) while propagating through several stages. Still, they managed to operate up to 64-bitsdue to their internal design structures. With careful in section of Fig. 3.1, it can be observed

that in each stage, An and Bn terms are inserted as fresh inputs. The carry term needs to propagate through several stages. In the existing design s, since the input carry term Cin is used as gate control of the TGs, the possible signals which might appear at the output terminal (Cout terminal) are Vdd, Gnd or B. If we consider only B (since Vdd and Gnd will be provided as fresh inputs in each stage), for n=0, B0 will appear in the output terminal (C1output terminal) whereas for n=1, B1 will appear in output terminal (C2 output terminal).

Modern electronic devices demand faster operation and longer battery life with minimum layout footprint. However, silicon area and power dissipation are inversely proportional to the computing speed. Therefore, circuit designers need to make trade-offs to meet the system demand.

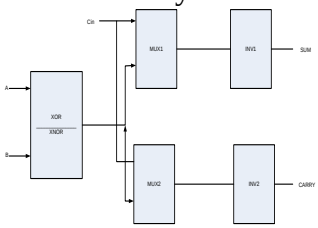


Figure 6. Block Diagram Of Proposed Hybrid Full adder Design

5) XOR-XNOR-Based Hybrid Full Adder Design

The proposed XOR-XNOR module and the corresponding circuit diagram is shown in Fig. 3.2a. For different input-output patterns, the operation of the proposed XOR circuit can be understood as follows:

Input Pattern AB =00: XORoutput =B =0 (since B =0); for this input combination, p3 transistor is ON, n1 and n2 transistors are OFF. Through p3, strong logic 1 is passed on to the intermediate node IND. As a result, IND =1 switches ON n3 which causes XOR output to go down to strong logic 0 because of input B =0. In addition to this, p1 and p2 transistors are ON through which weak zero is passed towards XOR output. Since n3 is providing strong logic 0 for input pattern AB =00, the XOR output will be strong logic 0 for this case. Input Pattern AB =01: XOR output =B =1 (since B =1); for this input combination, p2 transistor is ON (since input A =0), and XOR output is pulled up to strong logic 1 because B =1. Moreover, p3 is ON for this input pattern by which strong logic 1 is passed on to the intermediate node IND. As a result, n3 is switched ON and passes weak logic 1 to the XOR output. Furthermore, B =1 switches ON n1 through which weak logic 1 is passed on to the XOR output. Input Pattern AB =10: XOR output =A =1 (since A =1); for this input combination, p1 transistor is ON (input B =0) and XOR output is pulled up to strong logic 1 because A =1. Input Pattern AB =11: XOR output =0; for this input combination, n1 and n2 transistors are ON (since inputs A =B =1) and XOR output is pulled down to strong logic 0. Similarly, the Input Pattern AB =00: XNOR output =1; for this input combination, p3 and p4transistors are ON (inputs A =B =0). Through p3 and p4, XNOR output is pulled up to strong logic 1. Input Pattern AB =01: XNOR output =A =0 (since A =0); for this input combination,n5 transistor is ON (input B =1) and XNOR output is pulled down to strong logic 0 because A =0. Input Pattern AB =10: XNOR output =B =0 (since B =0); for this input combination,n4 transistor is ON (input A =1) and XNOR output is pulled down to strong logic 0 because B =0. Moreover, A =1 turns ON n2 and the intermediate node IND is pulled down to strong logic 0. This IND =0 turns ON p5 through which weak logic 0 is passed towards the XNOR output. Furthermore, B =0 turns ON p4 through which weak logic 0 is passed towards the XNOR output. However, there is at least one transistor path (n4) that provides strong logic 0 to the XNOR output. Therefore, for the input pattern AB =10, the final XNOR output will be a strong logic 0. Input Pattern AB =11: XNOR output =1 (since B =1); for this input combination, n2 transistor is ON and p3 and p4 transistors are OFF. As a result, strong logic level 0 is passed on to the intermediate node IND through n2. This IND =0 switches ON p5 which causes XNOR output to be pulled up to strong logic 1 because of input B =1. Moreover, n4 and n5 transistors are ON for AB = 11 which provides weak logic 0 towards the XNOR output. But, since n2 provides strong logic 0, the final XNOR output for AB =11 is weak logic 0. Table provides a complete summary of the full swing and non-full swing transistor paths for all possible input combinations of the XOR-XNOR module. From the

Table, it can be seen that for each input pattern, there is at least one transistor path that can provide full- swing output without any threshold voltage drop issue. As a result, the proposed hybrid XOR-XNOR produces full swing output.

6) Sum Generation Circuit

With careful observation of the input-output logic levels of Sum in Table 1, the following set of conditions are required to implement the Sum generation circuit

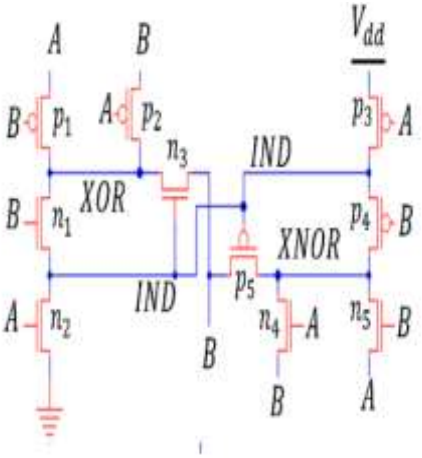


Figure 7 Proposed XOR-XNOR Circuit.

For implementing the conditions mentioned above, a 2:1 Multiplexer (2:1 MUX) based on Transmission Gate (TG) has been used. In Fig. 3, TG1 (comprised of n6 and p6) and TG2 (comprised of n7 and p7) are used to implement 2:1 MUX for the Sum generation circuit. Since TG can pass strong logic 0 and strong logic 1, the Sum generation circuit will provide full swing output.

7) Carry Generation Circuit

The carry generation module, as shown in Fig. 3, is considered the most important part of FA since the scalability of a FA design depends highly on the signal strength of the carry-out signal (Cout). In wide word length adders, the Cout of one FA stage is utilized as the Cin signal of the next stage. Therefore, the Cout signal of FA needs to have ample drive power and the voltage level needs to be replenished.

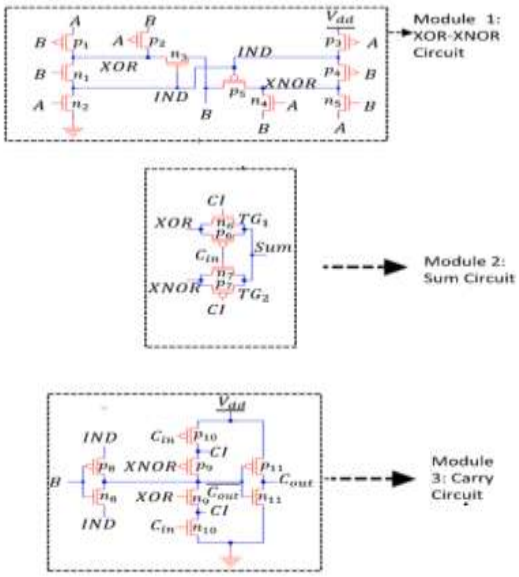


Figure 8. Proposed Hybrid FA Circuit

For this reason, the proposed Cout circuit consists of CCMOS logic-based inverter at the output terminal which consists of a pull-up transistor p11 and a pull-down transistor n11. In the case of CCMOS logic, the output terminal is either connected to Vdd (pull-up transistor p11) or connected to Gnd (pull-down transistor n11) for which the output voltage level of the proposed In addition, CCMOS logic provides adequate driving power to the circuit. Moreover, the inverter at the output reduces the carry chain delay due to the presence of only one pull-up and pull-down transistors. Input patterns AB =00 or AB =11: Cout =IND, $\overline{Cout}$ =IND. For AB =00 combination, p8 and n11 transistors are switched ON. PMOS p8 provides strong logic 1 to the gate of n11 since IND =1 for this case. This turns ON n11 by which the Cout output is pulled down to strong logic 0. On the other hand, for AB =11 combination, n8 and p11 transistors are switched ON. NMOS n8 provides strong logic 0 to the gate of p11 since IND =0 for this case. This turns ON p11 by which the Cout output is pulled up to strong logic 0. The carry output Cout is independent of Cin for these patterns (AB =00 or AB =11). Input patterns Cin =0, AB =01or AB =10: Cin =0 and XNOR =0 (for AB =01/10, XNOR =0) will switch ON p10 and p9. Therefore, the Cout node will be pulled up to '1' through p10,p9. This Cout =1 will switch ON

n11by which Cout will be pulled down to '0'. Input patterns Cin =1, AB =01or AB =10: Cin =1 and XOR =1 (for AB =01/10, XOR =1) will switch ON n10 and n9. Therefore, the Cout node will be pulled down to logic '0' through n10 and n9. This Cout =0 will switch ON p11 by which Cout will be pulled up to '1'.

IV. RESULTS AND DISUCSSIONS

1) Existing Hybrid Full adder Design

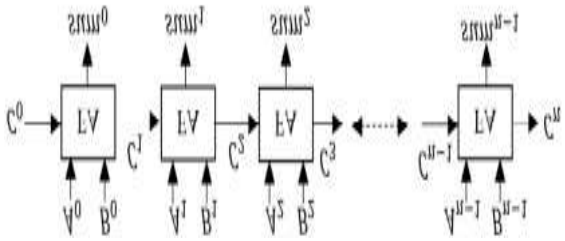


Figure 9 Implementation of n-bit adder using 1-bit FA

Hybrid FAs and the proposed design do not incorporate CCMOS logic in the output terminals. Still, they managed to operate up to 64-bits due to their internal design structures. With careful inspection of Fig. 4, it can be observed that in each stage, An and Bn terms are inserted as fresh inputs. The carry term needs to propagate through several stages. In the proposed design, since the input carry term Cin is used as gate control of the TGs, the possible signals which might appear at the output terminal (Cout terminal) are Vdd, Gnd or B. If we consider only B (since Vdd and Gnd will be provided as fresh inputs in each stage), for n=0, B0 will appear in the output terminal (C1 output terminal) whereas for n=1, B1 will appear in output terminal (C2 output terminal). Hence, the same signal does not propagate through n=0 to n=63 for which the design is not subjected to voltage degradation when extended to wide adder, To test drive capability of the proposed FA design, a wide range of output loads from fan-out of 4 unit-size inverters (FO-4) to fan-out of 64 unit-size inverters (FO-64) have been applied. The supply voltage for this case was set to 0.8 V.

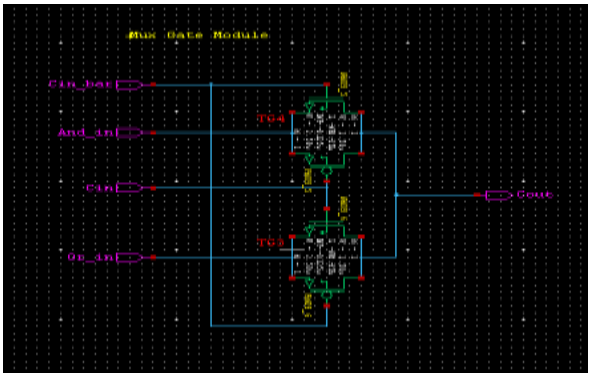


Figure 10 Proposed Hybrid Full adder Design

Channel widths are selected in an appropriate manner in order to ensure optimal performance. Average Power Consumption (APC), Propagation Delay (PD) due to the critical path, Area Delay Product (ADP), and Power Delay Product (PDP) are the major parameters that have been used to compare the performance of FAs. Finally, APC is determined by taking the average of the previously calculated power dissipations. The power consumption occurred due to the output side FO4 inverters and the input side buffers are not taken into consideration while calculating the APC of a FA cell. In CMOS circuits, different input patterns result in different PDs. However, there exists one delay path for which the maximum PD occurs. This delay path is known as the critical path delay or worst-case delay path. For PD calculation in this research, critical path PD has been considered. The PDP is obtained by multiplying critical path PD by APC. The ADP design metric is computed by multiplying the Area with the PD.

2)Block Diagram of Proposed Hybrid Full Adder design

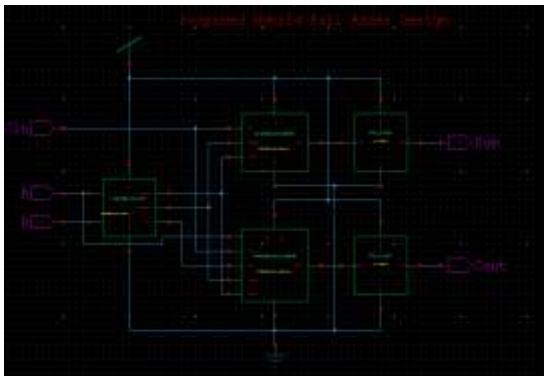


Figure 11 circuit Diagram Of Proposed Xor - Xnor Module

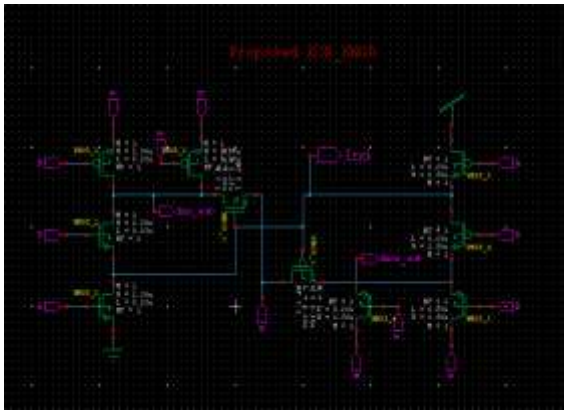


Figure 12 circuit Diagram Of Proposed Xor - Xnor Module

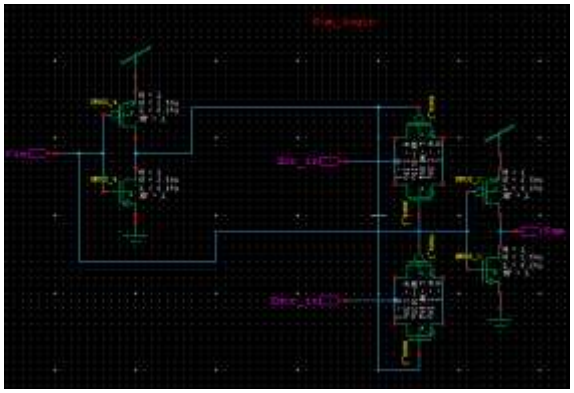
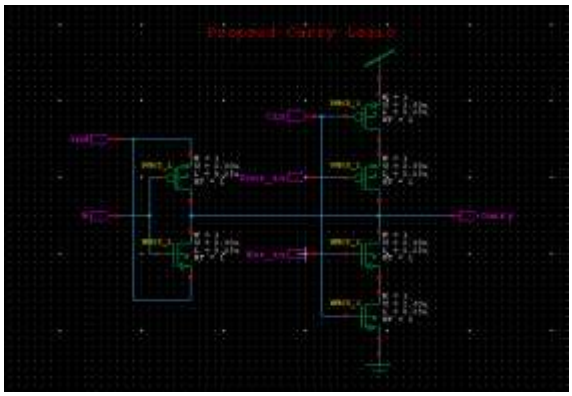


Figure 13. Circuit Diagram Of Proposed Sum Module

3)Circuit Diagram Of Carry module



4)Output Results

A. Power report

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Power Results

V1 from time 0 to 1e-007
Average power consumed -> 1.037762e-005 watts
Max power 4.401043e+000 at time 8.0002e-008
Min power 1.065372e-009 at time 2e-012
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Figure 14 Proposed method

B. Simulation Output wave form

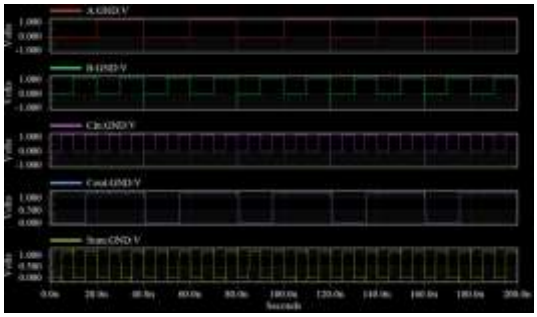

Figure 15. Power report

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Power Results

V1 from time 0 to 2e-007
Average power consumed -> 4.460878e-005 watts
Max power 1.374083e+000 at time 1.20002e-007
Min power 1.743924e-009 at time 5.0005e-009
```

Figure 16. power report summary

Table.1.Comparsion results

S.No	Parameters	Existing hybrid Full Adder Design	Prposed hybrid Full Adder Design
1	Aveage Power in Watts	1.037e-005	4.46e-005
2	Delay in ns	2.25	3.58
3.	Transistor Count	22	20

V. CONCLUSION

A full-swing hybrid FA implementation using the XOR-XNOR module is implemented. The FA design has been implemented using Tanner design and simulation tools. A comparative analysis of existing and proposed FAs has been presented. Compared to the conventional CCMOS FA, the proposed FA exhibits improvement in silicon area, improvement in Average Power, 33% and 12% improvement in Propagation Delay. The scalability of existing and proposed FA designs in wide word-length architecture has been investigated by extending the designs to 4-bits. When extended to a 32-bit configuration, the per-centage of improvements are 22.4% in Average Power, 31.24% in Propagation Delay, and 8.58% in PDP, when compared to the CCMOS FA.

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