Hybrid Redundancy Approach for High Speed Trains Using FPGA

Sangeetha Arumugam, Vinu Ganeshan, Karthick S

***Abstract*—**The development of the railway technology, as a leading transportation technology, requires more and more efficient, intelligent and faster subsets. High speed trains, which are the heart of the railway transportation, play a major role in this field. To achieve a reliable and safe high-speed transportation system, the intelligent controllers are always preferred to human supervisor. In order to realize intelligent controllers, beside the processors, the field programmable gate arrays (FPGAs) can be used. The FPGAs are interesting due to low non-recurring engineering (NRE) costs, their reconfiguration capability, and computational efficiency benefits over general purpose processors. A very complex control algorithm can be implemented in to FPGA and its run-time can be considerably reduced based on parallel processing hardware circuit. In the proposed Hybrid Dual Duplex Redundancy (HDDR) method, the original controller is quadruplicated and correct values are voted through the comparator and error detection unit. We have analyzed the proposed system with Reliability, Availability, Mean time to failure and Security theory in order to evaluate the effectiveness of proposed scheme

***Keywords*—** Field Programmable Gate Arrays (FPGAs); Hybrid Dual Duplex Redundancy (HDDR); Fault tolerant system; Reliability; High speed railway

I. INTRODUCTION

A high-speed train is one intended for regular operations at speeds of over 200 km/h (125 mph), with a high level of service, and generally comprising multi-powered elements. Standard hauled trains, often able to reach 200 km/h, such as French Co-rail or German IC trains, unconventional trains, such as maglev and trans rapid, and prototypes are excluded High-speed rail is a type of rail transport that operates significantly faster than traditional rail traffic, using an integrated system of specialized rolling stock and dedicated tracks. The first such system began operations in Japan in 1964 and was widely known as the bullet train. High-speed trains normally operate on standard gauge tracks of continuously welded rail on grade-separated right-of-way that incorporates a large turning radius in its design.. As a result, we have been involved in developing a new train control system that satisfies these users and system needs.

Sangeetha Arumugam is with Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology,Sathyamangalam.

Vinu Ganeshan is with Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology,Sathyamangalam.

Karthick S is Assistant professor, Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology,Sathyamangalam.

High-speed trains, a hot topic among all transportation patterns, produce considerable social and economical benefits. High speed, on the other hand, means more dynamic actions and potential danger. Any transportation mode has speed limit, which is closely linked to the technical conditions of the time. For example, the travel speed of cars was able to double owning to the emerging of high-speed highway system. Similarly, a plane can reach the speed of 1000 km/h only when it fly's 10 000 meters above the sea level. In October 1964, in Japan, the first high-speed railway line in the world was put into operation, and the surpluses of Japanese railway ministry increased right in that year. Since then, the high-speed railway has experienced prosperous development. The high-speed trains, designed for rapidity, efficiency, energy conservation, security and comfort, give vitality to the traditional railway transportation. Railway transportation has entered into the era of high speed

II. OVERVIEW OF FPGA

Recently, Field Programmable Gate Arrays (FPGAs) have been increasingly used in many applications. The programmability of FPGAs has helped to achieve a short design cycle and low development costs, as well as a reduced time-to-market. FPGAs are widely used in different applications such as networking, digital signal processing, high performance computing, rapid prototyping and hard-ware emulation.

The programmability and modularity of an FPGA are readily adaptable to fault tolerance. Usually only a small portion of interconnect resources is used; when a fault occurs, in some cases it is possible to remap the design in the FPGA to bypass the faulty resources, so that the desired circuit can still function correctly. The availability and flexibility of the interconnect resources often determine whether it is possible to successfully reconfigure the FPGA with minimum performance penalty. Therefore, fault tolerance of different FPGA architectures and their resources such as the interconnect, must be evaluated. The switch block structure plays a significant role for routing and flexibility of reconfiguration.

In this paper new methods for establishing fault tolerance of FPGA switch blocks are proposed. The impact of faulty switches on the probability to route (routability) in a switch block is assessed. Rout ability is established as the existence of realizable permutations between the input and output endpoint sets. The impact of switch stuck-open faults (switch permanently off) as well as switch stuck-closed faults (switch

permanently on) are addressed, which is directly related to fault tolerance of the interconnect for testing and reconfiguration at manufacturing and run-time application.

A probabilistic approach is also proposed to evaluate fault tolerant routing for connecting switch blocks in chains as required for testing and to account for the I/O pin restrictions of an FPGA chip. This is complementary to previous works which focused on arranging the FPGA interconnect into specific configurations and apply vectors to test or diagnose to meet a specified fault cover-age or for successfully reconfiguring FPGAs to achieve fault tolerance.

The presented metric for routability is evaluated for commercial FPGA architectures, as well as academic FPGAs. The fault tolerance capabilities of these FPGA architectures are also compared.

The evolution of the technology, providing ever smaller and faster devices, is at the same time bringing new challenges to the design of fault tolerant systems. The higher sensitiveness of those new devices to radiation induced transient faults, a long time concern for space and mission critical applications, makes the detection and correction of transient errors also a mandatory issue to be considered even in the design of general purpose systems used at sea level. Moreover, the effects of single event transients (SETs) on combinational logic are now becoming a design concern as important as those of single event upsets (SEUs) affecting memory devices.

In parallel, the increasing availability of field programmable devices that include commercial off the shelf (COTS) processor cores makes this type of device the ideal platform for several applications. Their low cost and design flexibility are key factors to provide competitive products with shorter time to market

III. Field Programmable Gate Array

Many techniques have been proposed in the technical literature for repairing FPGAs when affected by permanent faults. Almost all of these works exploit the dynamic reconfiguration capabilities of an FPGA where a subset of the available resources is used as spares for replacing the faulty ones. The choice of the best reconfiguration technique depends on both the required reliability and on the architecture of the chosen FPGA . This paper presents a survey of these techniques and explains how the architectural organization of the FPGA affects the choice of a reconfiguration strategy. Subsequently, a framework is proposed for these techniques by which a fair comparison among them can be assessed and evaluated with respect to reliability. A reliability evaluation is provided for different repair strategies. To provide a comparison between these techniques FPGAs of different size are taken into account. Also the relationship between the area overhead and the overall reliability has been investigated. Considerations about time to repair and feasibility of these techniques are provided. The ultimate goal of this paper is therefore to present a state of the art repair techniques as applicable to FPGA and to establish their performance for reliability.

A. Programmable devices

Programmable devices, such as programmable logic arrays (PLAs), have been available since the 1970s. How-ever, for a number of years, their use was quite limited, mainly due to technological reasons. In the early 1980s, programmable array logic devices (PALs) started to be used as glue-logic parts but suffered from power consumption problems. The extension of the gate array technique to post manufacturing customization, based on the idea of using arrays of custom logic blocks (LBs) that are surrounded by a perimeter of I/O blocks, all of which could be assembled arbitrarily, gave rise to the FPGA concept, which was introduced by Xilinx cofounder Freeman and depicted in, which was founded in 1984, consisted of 85 000 transistors (no more than 1000 equivalent gates) and was fabricated in a 2-μm process. The continuous increase in price for application-specific integrated circuit (ASIC) flows in the 1980s, combined with the advance in semiconductor to ASICs as well as a solution for rapid system prototyping. However, they did not provide enough hardware resources, and software tools had not yet enough maturity to create optimized designs. FPGAs were slowly gaining popularity, but still they could not be used for

It is in the 1990s when the FPGA space reached a level of maturity that made them the choice of implementation in many fields. The late 1990s really opened the door to new FPGA applications. Devices and tools became powerful enough to deal with most designs. The FPGA industry made an effort to bring together IP, software, and hardware resources that enabled important advances in fields such as communications or signal processing. By 2004, Xilinx ranked as the fourth largest ASIC supplier.

Cost reduction has played a fundamental role in the development of FPGA technology. From 1990 to 2003, there has been a 10 000% reduction in the cost of the basic FPGA building block, consisting of one lookup table (LUT) and one flip-flop. Data (taken from the webcast presentation of Altera's CEO J. P. Daane at Lehman Brothers Global Technology Conference on Dec. 6, 2006) show how programmable devices, particularly, FPGAs, are increasingly dominating the logic IC market.

B. hardware point of view

From a hardware point of view, the new nanometerscale fabrication processes allow devices containing several million equivalent gates to be fabricated. An increasing number of logic and I/O resources are available, including complex manufacturing, made FPGAs a more appealing vehicle for an increasing number of applications, to

From a software point of view, new tools that allow the design to become increasingly hardware-independent have been developed (e.g., Xilinx' System Generator, which allows Simulink behavioural descriptions to be used as design entry). The design effort is also being dramatically reduced with the availability of software cores and IP blocks, which allow the time-to-market of FPGA-based designs to be shortened.

The practical applications nowadays are limitless. FPGAs are used virtually everywhere for different reasons [e.g.,

electronics for later upgrade and intellectual property (IP)]. New fields are being explored, such as, for instance, the design and validation of fault tolerant systems.

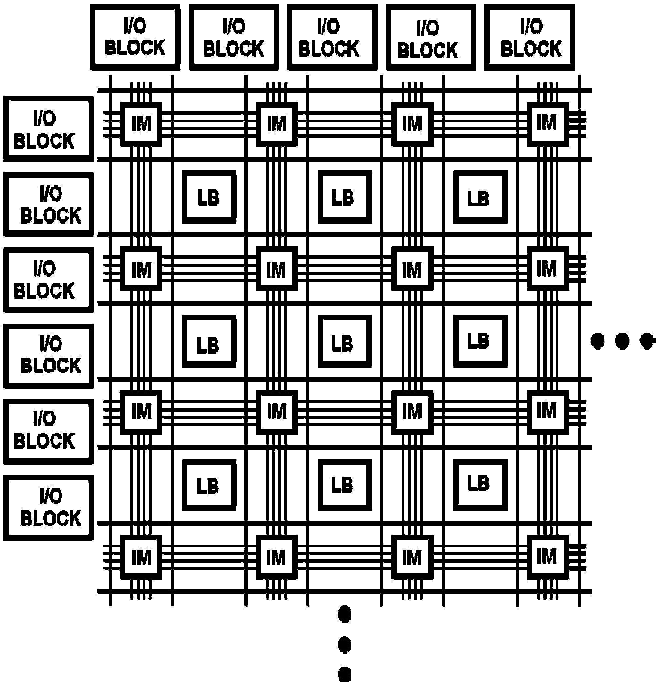

Fig. 1. FPGA concept (IM: interconnect matrix).

The extent that they started becoming an actual alternative functional blocks as, for instance, memories, phase-locked loops (PLLs)/delay-locked loops (DLLs), communication interfaces, or arithmetic circuits. Devices consisting of as much as eight million gates, providing up to 1000 user I/O pins, and reaching operating frequencies of up to 500 MHz are available. In addition, partial reconfiguration is a very promising issue that is addressed by recently developed devices. Another important factor to take into account is the availability of affordable but still powerful devices, such as, for instance, those of the Xilinx' Spartan and Altera's Cyclone families. Maybe the most impressive consequence of the features that are currently provided by state-of-the-art FPGAs is their ability to allow system-on-chip (SoC) solutions to be readily implemented.

IV. Fault Tolerant in High Speed Train

The interconnect resources of an FPGA consist of horizontal and vertical routing channels as well as programmable switch blocks which are used to connect the channels. In current FPGAs, almost of the area is devoted to interconnect resources, hence many papers have addressed testing and diagnosis of these resources. Application-independent testing of routing resources in FPGAs has been addressed. Diagnosis of interconnect faults in FPGAs has been discussed.

A. Fault Detection

The programmability of FPGA can also be used for fault tolerant applications, a comprehensive approach to reconfigure one-time programmable FPGAs with faulty logic resources has been proposed. In methods for tolerating faults in the FPGA logic resources by shifting the configuration data are presented. In a column-based reconfiguration technique using precompiled configurations is presented.

However, previous work can not be used to establish and assess the most appropriate switch structure for fault tolerance very little work has been reported under which conditions a certain configuration is realizable in the FPGA when faults are present. This effectively differentiates the switch block structures currently available from different manufacturers and their ability to provide routing when switches are faulty. In this paper we propose methods to evaluate fault tolerance in arbitrary switch block structures.

B. Approach and Algorithm

First consider the problem of determining whether at least a permutation can be found in a single fault-free switch block. The switch block is modeled as a bipartite graph.

The partition represents the input end points, the partition represents the output endpoints. Only the programmable switches between the two partitions (switches between input and output endpoints) are included into the bipartite graph model. Assume that as in practice, a switch block has the same number of endpoints for each port. A switch block can also be modeled as a matrix.

V. Automatic Train Control protection

The growing traffic intensity and complexity of the railway systems as well as the demand for higher speed need to new Automatic Train Control (ATC) methods. The conventional ATC system has some problems and in recent years new ATC methods like the Decentralized ATC (D-ATC) and autonomous decentralized ATC are developed which have some advantages. In this paper, an Intelligent Decentralized ATC (ID-ATC) approach based on the Multi-Agent systems theory is developed which can provide high transportation capacity, high-safety and high-reliability. In this method we combine the concept of cooperative systems theory with Multi-Agent control theory by using of fuzzy control logic. The control algorithms are presented and by using of simulation results the effectiveness of the method is demonstrated.

A. ATC Operation

Automatic control systems and their affects to reduce the human error problems are more attractive in recent years to control the railway transport systems due to the growing traffic intensity and complexity of these systems. Automatic Train Control (ATC) system is an automatic control algorithm to protect the trains from collision. In addition to collision avoidance, by using of the ATC system the following items can be achieved:

1. Improve the performance of control and signalling systems
2. Increase the safety

3. Reduce the costs
4. Reduce the energy consumption

According to the ATC definition, an ATC system consists of Automatic Train Protection (ATP), Automatic Train Operation (ATO) and Automatic Train Supervision (ATS). In figure 1, the fundamental structure of a typical ATC system which contains the ATP, ATO and ATS is shown. There are many kinds of ATC systems but in all of them, the ATP helps to prevent collisions through a driver's failure to observe a signal or speed restriction. The ATO provides partial or complete automatic train piloting and driverless functions and the ATS which is the basis of the train protection function and the automatic speed control devices. The ATS system, by using of the block information, specifies the speed constraints and sends them to the trains by using of Track circuit, Loop and/or Balises.

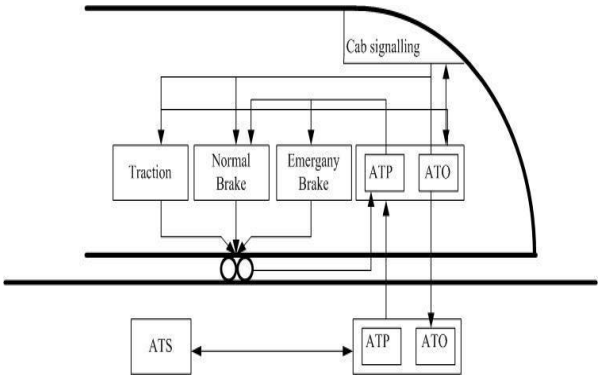

Fig 2. Structure of an Automatic Train Control (ATC) System

The recent advances in railway industries and high traffic intensity need to automatic control systems to reduce the human error problems. In last decade, some new algorithms were introduced in ATC systems which can be summarized in following titles:

1. D-ATC
2. DS-ATC

These new methods have some advantages and drawbacks in comparison with the conventional ATC algorithm. In the D-ATC was introduced and they claimed that it can solve some problems and reduce complexity of the conventional analogue ATC method. Also, this method can improve the ride quality, increase the line capacity and reduce the costs by using of decentralized topology. Advantages of the D-ATC approach results in some new algorithms.

B. Automatic Train Control Based On Intelligent Decentralized Control

In this paper, we introduce a new ATC method by using of Voronoi algorithm in cooperative systems theory. In 2004, Magnus Lindhe introduced the Voronoi algorithm by combining the Ogren effect of Navigation function and Cortes effect of Coverage Control to navigate a group of mobile robots. Voronoi algorithm by using of a potential function and by finding the smallest path to achieve the goal presents a safe method to run the mobile robots. In this approach, a Voronoi diagram is defined as figure 3 that guarantee the collision avoidance.

Here, we combine the Voronoi algorithm and Multiagent control systems by employing the fuzzy logic controller to present an intelligent ATC system which contains the D-ATC advantages and we call it ID-ATC. The ID-ATC can solve the problems of railway transport systems by defining the trains as agents and by using of the decentralized fuzzy controllers. In other words, each agent contains a fuzzy controller which receives the information from receptors and by analyzing them and considering the Voronoi conditions generates a control policy. In this procedure and in railway transportation system, distances between the current train and front and back trains are measured and by using of this information the decision making will be done to keep the current train in the middle point, which can guarantee the safe motion of the trains.

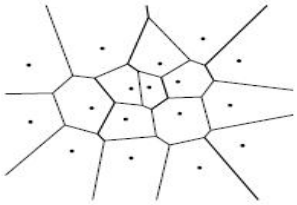

Fig.3 Voronoi diagram

C. ID-ATC Algorithm

In ID-ATC, we consider each train as an agent. Also, we consider the first train as a leader that the other agents adjust their position and consequently their velocity with the leader. In this section, we consider three trains in a line and between two stations to simplify the algorithm discussion but without any loss of generality of the problem. These three trains start the motion from the first station and stop in the last station respectively. Obviously, the number of trains is more than three in real states and to solve this problem, all trains without 1st and last trains can be considered as middle trains.

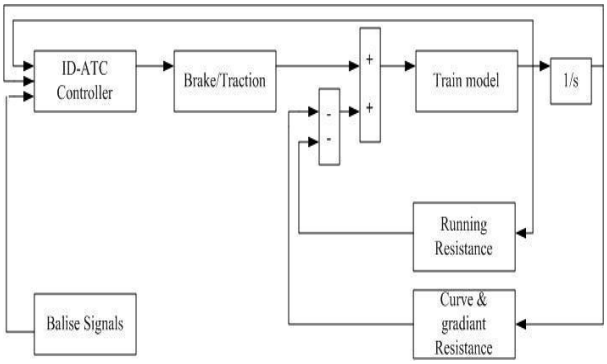

Fig.4 closed loop control system

In ID-ATC system, we propose the decentralized control structure and consequently we consider a controller for each train. The train controller plan by using of fuzzy strategy is shown in figure 3. In control procedure, each train receives the

position and velocity of itself and previous and next trains. After this phase, the controller provides the appropriate control effort to control the train velocity and position. In real train control systems this control effort specifies the notch of traction system or brake system.

In figure 4, the closed loop control system for a train is shown. This control loop contains the train dynamic model and resistance forces as running resistance and curve and gradient resistance. Also, in this closed loop control system we consider a controller to control the train velocity and position by using of the torque control strategy. According to Voronoi algorithm, this controller should keep the 2nd train in the middle point of two other trains to obtain the safe railway transportation system. But, in this control procedure we have some constraints as

1. The maximum speed of the trains should be specified.
2. Trains can not go back.
3. The control system of each train is independent of the others.

In ID-ATC, the 1st train is assumed as leader agent and its desired velocity should be specified by the control center. The fuzzy control system in each train receives the velocity and position of the previous and next trains. By using of this information, the ID-ATC present the control strategy to keep the 2nd train in the middle point between the leader and 3rd trains. This methodology can provide safe and intelligent railway system while it improves the ride quality.

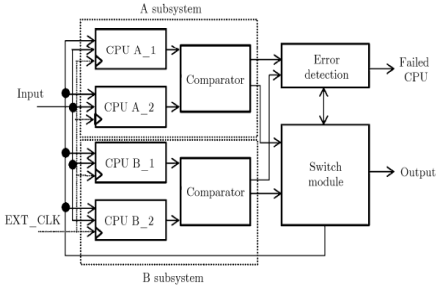

Fig.5.Block diagram of HDDR system

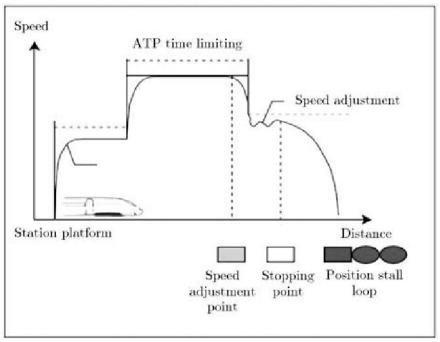

Fig.6 ATO Operation

D.Fuzzy Controller Design For Id-Atc System

In ID-ATC system we should design a fuzzy controller for each train. So, we can categorize the fuzzy controllers in 3 groups, controller of leader train, controller of middle trains and controller of last trains. The fuzzy controller design for the leader train is trivially simple and we ignore it to present. The controller of leader train receives the desired velocity from control center and adapts its velocity by employing the fuzzy controller. But, in the middle trains the fuzzy controller is more complex than the other controllers.

VI. HYBRID REDUNDANCY APPROACH

High-speed trains which provide rapidity, efficiency, security, and comfort have a considerable superiority to the traditional railway transportation. However, the high-speed train motion and operation is a complicated process, involving locomotive dynamics, communications and signalling, rail track considerations, and automatic speed controller. On the other hand, high speed means more dynamic actions and potential danger to safety. So there is a need to more reliable Automatic Train Operation (ATO). ATO involves speed regulation and controlling train speed, within the constraints of over-speed protection pattern, to make the run according to schedule speed regulation. The high safety and efficiency of the railway systems are mainly depended on the train speed controller systems. So, the train controller system because of controlling train's speed and routes is a vital system in railroad systems. This system senses and processes information, makes decisions, and transmits commands, and hence, the reliability of this part is a major problem in Automatic Train Control (ATC) process.

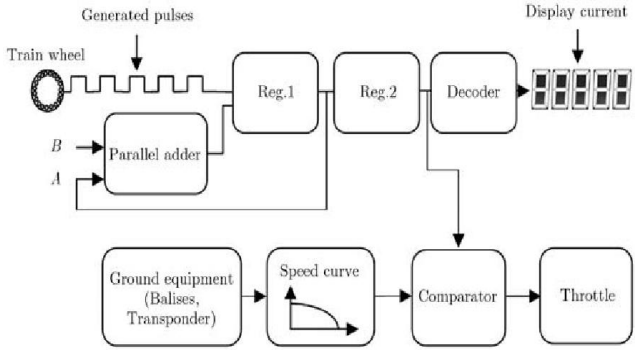

Fig.7 high speed controller

To realize the intelligent speed controllers, be-sides the processors, the Field Programmable Gate Arrays (FPGAs) can be used. FPGAs are widely utilized in many applications such as high speed trains, aerospace and avionics, networking, signal processing, and fault-tolerant computing, due to their high efficiency, low Non-Refundable-Engineering (NRE) cost, and fast time-to-market. Also, they can implement the behaviour of any digital module practically, which is a desirable specific for designers and construct a complex sequential logic circuit.

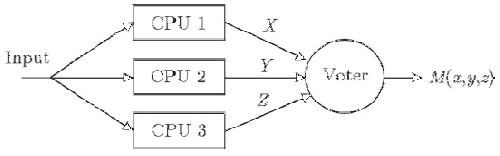

Fig. 8 TMR structure

However, the use of such devices for critical applications is being delayed by the deficiency of the effective techniques to mitigate some errors such as Electro-Magnetic Interference (EMI) induced errors. So the trend of the novel systems is toward a more quantitative form of specification, particularly for reliability, maintainability, and availability requirements. Therefore, the rules of safety and fault-tolerant systems have to be applied in such environments to prevent the occurrence of errors. For this purpose, fault tolerant techniques (*e.g.*, Triple Modular Redundancy (TMR)) have always been broadly used for high reliability applications, like transport, space, and avionic.

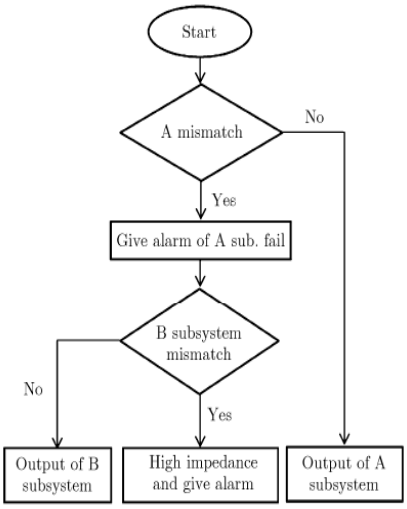

Fig:9 flow chart of HDDR structure

Some approaches for increasing the reliability of the train control system have been proposed. However, these works are mainly based on simulation results. In this paper, we propose a fault tolerant design and implementation of a high speed train controller system, whose basic structure was introduced. The purpose of this paper is to design an automatic train control sys-tem based on FPGA to manage the train speed in a safe way. The proposed scheme which is based on fault tolerant system techniques is able to improve the reliability of the speed controlling system against the possible faults, which affects the whole systems that have been implemented on FPGA. We called this scheme as Hybrid Dual Duplex Redundancy (HDDR) system and will compare this structure with other hardware redundancy approaches such as TMR and Selective TMR (STMR). Also, a prototype, whose correct operation has been confirmed by means of simulations and experimental measurements, has been implemented on a Xilinx FPGA.

To evaluate the dependability of the mentioned structures (plain, TMR, STMR, and HDDR), re-liability, availability, Mean Time To Failure (MTTF) and security analyses have been developed. Moreover, for evaluating the fault effects in practical system, we have used Single Event Upsets (SEUs) emulation technique on SRAM based FPGAs. Our platform, which is called as Dynamic Partial Reconfiguration based Fault Injection Platform (DPR-FIP), provides an appropriate setup that the user deliberately or randomly injects the single or multi upset in the configuration memory of SRAM FPGA. Theoretical analyses and experimental SEU injection results validate the efficiency of the proposed HDDR technique.

The reminder of this paper is organized as follows. In next section, we outline the proposed high speed controller system. The structural diagram of the HDDR has been introduced to analyze the reliability, availability and maintainability of the proposed structure in comparison with TMR technique. We describe the post-layout simulations and FPGA implementation results that used to verify the operation of HDDR structure.

A. High Speed Controller System

ATO as the main part of train automation includes several board computers. It involves speed regulation, controlling, and over-speed protection subsets. Also, ATO is responsible for all the traction and braking controls, as well as parking and stopping operations, as further illustrated. The speed controller as the core of ATO, firstly collects the track circuit information, train braking force, the slope of the line, train speed and other information, and then generates the barking pattern curves and compares it with the current train speed. Finally, if necessary, the speed controller will generate brake information through fail-safe circuit to make sure that the train is in a safe status. We have proposed and implemented an efficient speed controller for high speed trains. The architecture of this speed controller is shown.

The speed controller at first determines the current speed, and then compares it with the velocity limit which is received from the ground equipment. This comparison determines the permitted speed at any time and generates appropriate commands. The generated speed pattern is the most important base of continues controlling, such as ATC-S standard developed by Japan train control system. So, by the use of such information, the train's status will be safe.

B. Proposed Hybrid Dual Duplex Redundancy Structure

As we explained, this paper aims to provide a reliable structure for operating speed controller system for the high speed train. In order to increase the reliability of such systems, the duplex structure and TMR approach is widely used in fault-tolerant system. Duplex structure generally consists of two replicated units, while each one performs the same operation. Also, the TMR structure contains of three replicated units of the original circuit, while all of them provides the same function. In TMR system, a voter determines the overall output based on majority rules.

In the fault tolerant systems, totally, three versions of hardware redundancy are considered. Firstly, the static

hardware redundancy which is used for immediate failure masking, like TMR structure. Secondly, the dynamic hardware redundancy in which the spare components are activated is failed when the main active component. Finally, the hybrid hardware redundancy is a combination of static and dynamic redundancy techniques. The static hardware redundancy masks permanent and intermittent failures but its reliability drops below that of a single module for very long mission times. Also in dynamic hardware redundancy, all *N* spare modules are active (powered), and therefore the spare modules lifetime is decreased. However, a hybrid redundancy overcomes these drawbacks by adding the spare modules to replace the active modules as soon as they become faulty. In the proposed scheme, we have used two modules and two spares. Unlike the TMR version, which only can mask faults, the proposed structure in addition to fault masking capability, provides a fault detection signal for each replicated units to determine the faulty controller and replace it.

HDDR, consists of four speed controllers, two comparators, error detection component, and switching units. The speed controller units involve two subsystems, each of them includes two controllers. It is supposed that the system is hybrid redundant. This means that if one primary speed controller is failed, the other one can be used immediately. In HDDR scheme, a signal is used to determine the status of each speed controller. The status signals are transmitted to the error detection unit, to enable the other speed controllers for realize hybrid redundancy mode. The output of each subsystem is determined by the comparators. It is better to mention that all of the subsystems are independent and they also work concurrently.

VII. CONCLUSION

In this paper, we have proposed the fault tolerant design, implementation and measurement of the speed controller core for railway applications. The behavior of the proposed hardening technique, HDDR structure, has been verified by means of post-layout simulations and experimental measurements on a Xilinx Virtex 4 FPGA prototype.

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