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Design and Implementation Of Mobile Wimax (Ieee 802.16e) Physical Layer Using FPGA

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Abstract— Mobile WiMAX (IEEE 802.16e standard) is widely used for configuring wireless Metropolitan Area Network (MAN) which uses Orthogonal Frequency Division Multiple Access(OFDMA). Orthogonal Frequency Division Multiple Access is a multiuser version of the popular Orthogonal Frequency Division Multiplexing (OFDM) digital modulation scheme. FFT is one of the important blocks used in OFDMA systems. This paper presents implementation of a 1024-point Fast Fourier Transform (FFT) processor for Mobile WiMAX. Radix 2^2algorithm is proposed and used for the OFDM communication system. The design has been coded in VHDL and targeted into Xilinx Spartan 3 FPGAs.

Keywords - WiMAX, FFT, OFDMA, Radix 2^2 algorithm

I. INTRODUCTION

WiMAX is an emerging technology with significant potential and is poised to revolutionize the "broadband wireless internet access" market. The diverse hardware requirements including processing speed, flexibility, integration and time-to market necessitate an FPGA based implementation platform. OFDM is an attractive modulation scheme used in broadband wireless systems that encounter large delay spreads. Fast Fourier Transform (FFT) is one of the key components in an OFDM system. Nowadays, several communication systems require higher points FFT and higher symbol rates. This requirement establishes challenges for low power and high speed FFT designs with large number of points.

Pipelined architectures are further classified in two types: (1) SDF (Single Delay Path Feedback) (2) MDC (Multiple Delay Path Commutator). Both have their personal advantages. MDC utilization of delay elements is low in MDC as compared to SDF [2]. MDC uses more number of storage elements as compared to SDF.An efficient hardware oriented radix-2^2 algorithm is developed by integrating a twiddle factor decomposition technique. This is done by divide and conquer approach to form a spatially regular Signal Flow Graph (SFG). Mapping the proposed algorithm to the cascading delay feedback structure leads to the proposed architecture.

II. BASIC FFT ALGORITHM

The Discrete Fourier Transform (DFT) for an N-point sequence x(n)is given by (1), where X(k)and x(n)are complex numbers, n is the time index and k is the frequency index [1]. By using this equation the DFT computation requires N^2 complex multiplications and N(N–1) complex additions, leading to a complexity of $O(N^2)$.In [2] Cooley and Tukey proposed (actually they "rediscovered") an algorithm to compute the DFT with complexity O(N.log2N). Such algorithm, known as Fast Fourier Transform (FFT), is widely used in hardware accelerators. Direct hardware implementations of the FFT algorithm either use the Decimation in Time (DIT) decomposition or the Decimation in Frequency (DIF) decomposition [1], the latter used in this work. In the DIF approach an N-point DFT is decomposed into two N/2-point DFTs, one for the even-indexed frequency outputs and another for the odd-indexed frequency outputs. The inputs to the even-indexed outputs N/2-point DFT are sums between first half inputs and second half inputs. The inputs to the odd-indexed outputs N/2-point DFT are differences between first half inputs and second half inputs, multiplied by constants that are referred to as "twiddle factors". Each N/2-point DFT may be further decomposed into two N/4-point DFTs. Such decomposition may be applied recursively until reaching 2-point DFTs, which can be assumed as basic computation elements. Figure 1 shows in detail the signal flow chart (SFG) for an 8-point DIF FFT.

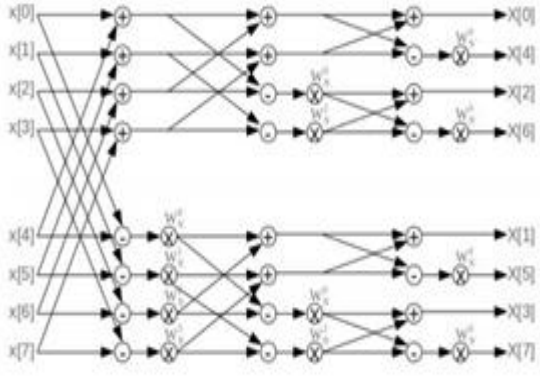

Figure 1 Signal flow graph for 8 point DIF FFT

A 2-point FFT processing element, normally referred to as "butterfly", is composed by one complex multiplication, one complex addition and one complex subtraction. Therefore, an N point FFT has $\log_2 N$ stages where each stage has N/2 complex multiplications, N/2 complex additions and N/2 complex subtractions, resulting in O(N.log2N) complexity, which is significantly lower than that of a direct implementation of (1).

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III. RADIX 2^2 FFT ALGORITHM

A useful state-of-the-art review of hardware architectures for FFTs was given by He et al. [3] and different approaches were put into functional blocks with unified terminology. From the definition of DFT of size N [6]:

$$X(K)=\sum_{n=0}^{N-1} x(n)\, W_N^{nk}, 0 \leq k < N \qquad (2)$$

where denotes the primitive Nth root of unity, with its exponent evaluated modulo W_N, x(n) is the input sequence and X(k) is the DFT. He [3] applied a 3-dimensional linear index map,

$$n = \left\langle \frac{N}{2} n_1 + \frac{N}{4} n_2 + n_3 \right\rangle$$
$$k = \left\langle k_1 + 2k_2 + 4k_3 \right\rangle_N \qquad (3)$$

and Common factor algorithm(CFA) to derive a set of 4 DFTs of length N/4 as

$$X(k_1+2K_2+4K_3) = \sum_{n_3=0}^{\frac{N}{4}-1} \left[H(k_1,k_2,n_3) W_N^{n_3(K_1+2K_2)} \right] W_{\frac{N}{4}}^{n_3 k_3} \qquad (4)$$

Where n_1,n_2,n3 are the index terms of the input sample n and k1,k2,k3 are the index terms of the output sample k .

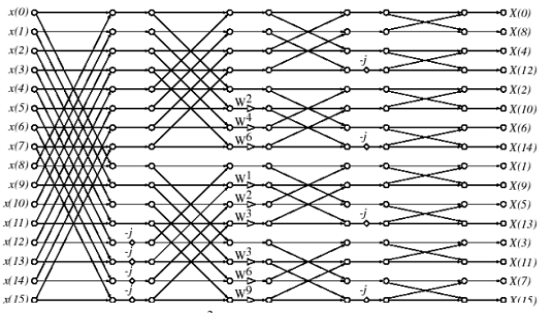

Figure 2 Radix- 2^2 DIF FFT Flow graph for N=16.

IV. RADIX 2^2 SDF FFT ARCHITECTURE

The more efficient architecture in terms of memory utilization is the delay feedback .The Radix-2^2SDF architecture is a hybrid of Radix-2 SDF and Radix-4 SDF designs. Radix-4 algorithm based single-path architectures have higher multiplier utilization ; however, Radix-2 algorithm based architectures have simpler butterflies and control logic. The radix 2^2 FFT algorithm has the same multiplicative complexity as radix 4 but retains the butterfly structure of radix 2 algorithm [7]. Starting from the radix-2 DIF FFT algorithm, first calculate the common factors at every odd stage and then move them to the next even stage at the right side. The FFT algorithm resulting from this procedure is exactly the same as the radix-2^2 algorithm if the property of $W_N^{N/4} = -j$ is applied. The Radix-2^2 algorithm not only reduces the computational complexity but also retains the simple structure of the radix-2 algorithm. The multiplicative operations are in a such an arrangement that only every other stage has non-trivial multiplications. This is a great structural advantage over other algorithms when Pipeline FFT architecture is under consideration. Although the overall signal flow is almost the same as the radix-2 algorithm, the number of stages requiring twiddle factor multiplication is reduced to half like the radix-4 algorithm. The Radix-2^2 algorithm is usually implemented by employing a butterfly pair accompanied with an additional multiplexer at every odd stage and a conventional one at every even stages. Butterfly Structure 1 can be implemented without a twiddle factor multiplier, the number of stages requiring twiddle factor multiplication is reduced to half. Therefore the Radix-2^2 algorithm leads to a more efficient hardware implementation .

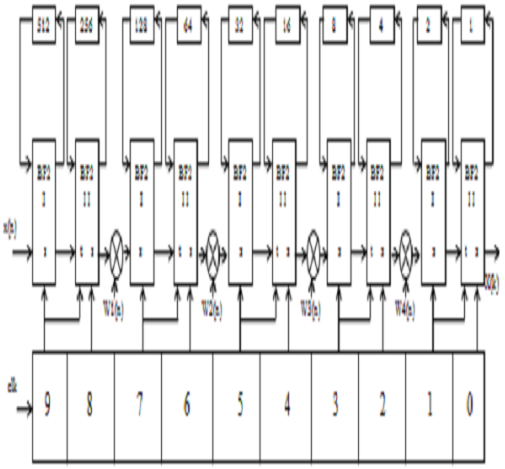

Figure 3 Proposed Radix-2^2 SDF FFT architecture

A) BUTTERFLY STRUCTURE I

The input Ar, Ai for this butterfly comes from the previous component which is the twiddle factor multiplier except the first stage it comes form the FFT input data. The output data Br, Bi goes to the next stage which is normally the Butterfly II. The control signal C1 has two options C1=0 to multiplexers direct the input data to the feedback registers until they filled. The other option is C1=1 the multiplexers select the output of the adders and subtracters. The process of the Butterfly I is to store the anterior half of the N point input series in feedback registers, than butterfly calculation when the posterior half data is coming, the result of the butterfly is Br, Bi, Dr, Di. Br, Bi fed to the output result of the Butterfly I the other result Dr, Di goes to the feedback registers.

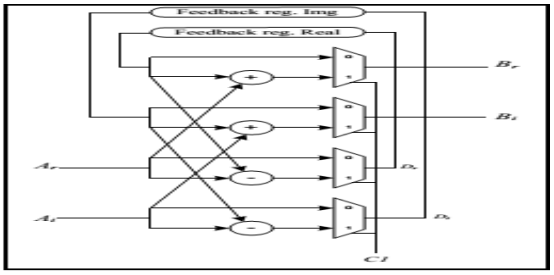

Figure 4 a) BFI structure

B) BUTTERFLY STRUCTURE II

The input data Br, Bi comes from the previous component, Butterfly I. The output data from the Butterfly II are Er, Ei, Fr and Fi. Er, Ei fed to the next component, normally twiddle factor multiplier. The Fr and Fi go to the feedback registers. The multiplication by –j involves swapping between real part and imaginary part and sign inversion. The swapping is handled by the multiplexers . Swap-MUX efficiently and the sign inversion is handled by switching between the adding and the subtracting operations by mean of Swap-MUX. The control signals C1 and C2 will be one when there is a need for multiplication by −j, therefore the real and imaginary data will swap and the adding and subtracting operations will switched.

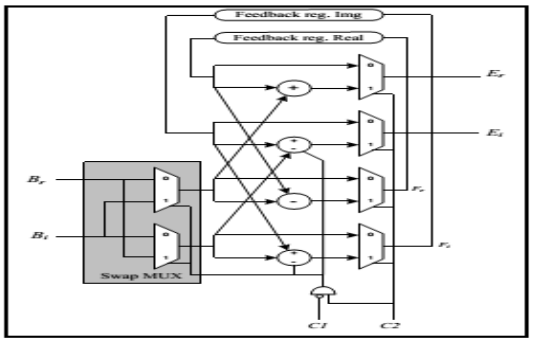

Figure 4 b) BFII structure

C) DELAY FEEDBACK STRUCTURE

In order to reuse the existing hardware, the delay feedback is used. The delay feedback architectures reorder the input by first accepting part of the data stream into the butterfly elements, but instead of computing on the block, it is redirected to a feedback delay line. By the time, the data appears again at the input of the butterfly.

D) CONTROL UNIT

Radix-2^2 control unit is simple. A $\log_2 N$ counter is used to switch the butterflies between modes. It also used as address to ROMs in order to pick the twiddle factors.

V. APPLICATION OF PROPOSED FFT IN OFDM SYSTEM

The standard for WiMAX technology is a standard for Wireless Metropolitan Area Networks(WMANs) that has been developed by working group number 16 of IEEE 802, specializing in point-to-multipoint broadband wireless access. WiMAX technology uses some key technologies to enable it to provide the high speed data rates. OFDM has been incorporated into WiMAX technology to enable it to provide high speed data without the selective fading and other issues of other forms of signal format. The fundamental principle of the OFDM system is to decompose the high rate data stream (bandwidth = W) into N lower rate data streams and then to transmit them simultaneously over a large number of subcarriers .

The IFFT and the FFT are used for, respectively, modulating and demodulating the data constellations on the orthogonal subcarriers. The transmitter and receiver blocks contain the FFT and IFFT modules. The FFT processor must finish the transform within the time to serve the purpose in the OFDM system. This FFT architecture effectively fits into the system.

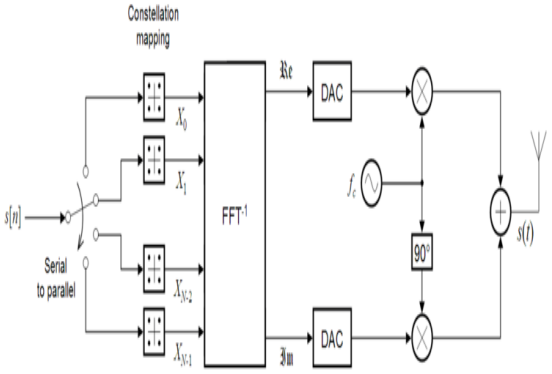

Figure 5 a) OFDM Transmitter

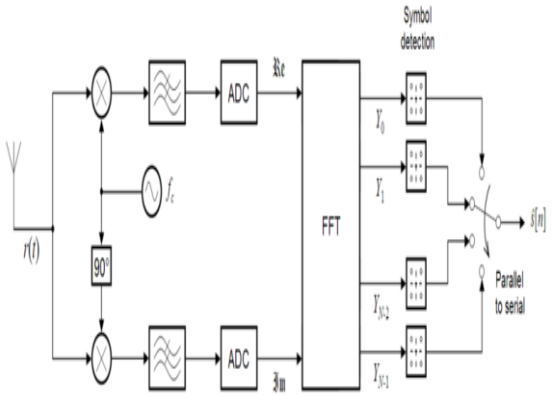

FIGURE 5 b) OFDM Receiver

An OFDM carrier signal is the sum of a number of orthogonal sub-carriers, with baseband data on each subcarrier being independently modulated commonly using some type of quadrature amplitude modulation (QAM) or phase-shift keying (PSK) . This composite baseband signal is typically used to modulate a main RF carrier. s[n] is a serial stream of binary digits. By inverse multiplexing, these are first demultiplexed into N parallel streams, and each one mapped to a (possibly complex) symbol stream using some modulation constellation (QAM, PSK, etc.). Note that the constellations

may be different, so some streams may carry a higher bit-rate than others.The receiver picks up the signal r(t), which is then quadrature-mixed down to baseband using cosine and sine waves at the carrier frequency. This also creates signals centered on $2f_c$, so low-pass filters are used to reject these. The baseband signals are then sampled and digitized using analogue-to-digital converters (ADCs), and a forward FFT is used to convert back to the frequency domain .

VI. SIMULATION RESULTS

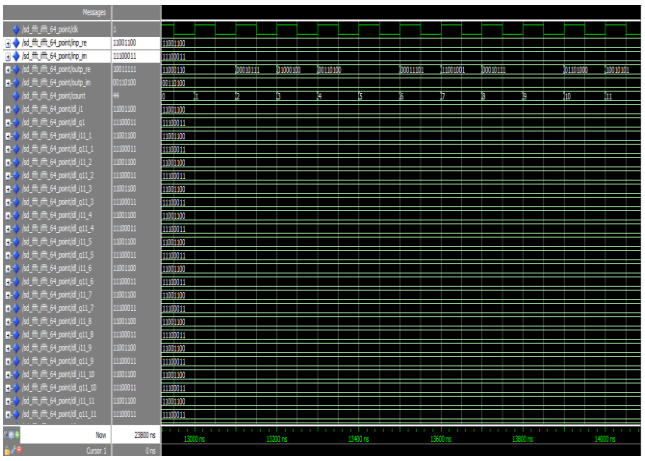

Figure 6 64 Point Radix 2^2 SDF FFT PROCESSOR

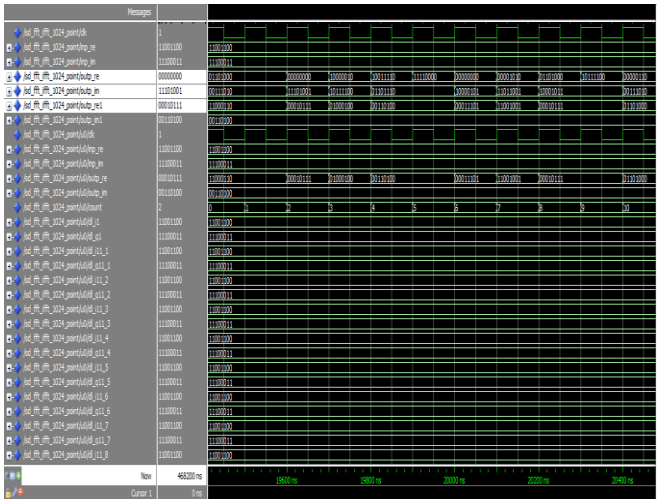

Figure 7 1024 Point Radix 2^2 SDF FFT PROCESSOR

VII. CONCLUSION

WiMAX are gaining a significant share in the broadband access service market. These standards are still in the early stages of development, and in field programmability as well as fast prototyping are essential for their development and deployment. In this work the FPGA based 1024 Point Radix 2^2 single-path Delay Feedback FFT processor are developed and simulated using MODELSIM SE6.4C.

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