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A VLSI Implementation of FIR Filter Based on VEDIC SUTRA & BEC Adder

Ms. Swetha V, Mr. P.Arunkumar

Abstract— *Finite impulse response (FIR) filters are used in Digital Signal Processing applications. Accuracy in Filter Designing is based on the Multiplication and accumulation of filter coefficients. This paper describes an approach to the VLSI implementation of digital filter which is flexible and provides superior to traditional approaches, low power, and area efficient Discrete Wavelet Transform architecture. A 4-tap finite impulse response (FIR) filter with two Vedic karastuba and BEC adder. Computation intensive applications such as DSP, image processing, floating point processors and communication technologies today require efficient binary multiplication which usually is the most power and time consuming block.*

This paper proposes an efficient design for unsigned binary multiplication to reduce delay. A 8x8 & 16×16-bit multiplier has been designed which is based on Vedic Karatsuba algorithm. It is optimized using adaptive and recursive approach combined with square-root carry-select-adder with BEC. The designs have been coded in Verilog, synthesized in Xilinx Tool and physically verified with Spartan 3 XC 3S 200 tq 144 platform.

Keywords— *Square Root Carry Select Adder, Karatsuba Multiplier, Wallace-Tree-Multiplier, Dadda-Multiplier, Recursive Adaptive Karatsuba Algorithm, Adder, Digital signal processing (DSP), finite impulse response (FIR) filter, Multiplier, Four tap Fir Filter, VLSI design.*

I. Introduction

In signal processing, the filter is used to remove some unwanted component or feature from a signal thereby improving the quality of signal. It alters the amplitude and/ or phase characteristics of a signal in a desired manner with respect to frequency. The primary function of filter are – to confine a signal into a prescribed frequency band, to decompose a signal into two or more sub-bands, to modify the frequency spectrum of a signal and to model the input output relationship of a system. Filters are extensively used in signal processing and communication system in applications like noise reduction, echo cancellation, image enhancement, speech and waveform synthesis etc. There are two main kind of filter: analog and digital filter. Analog filter has analog signal at both its input & output and are made up from components such as resistors, capacitors and op amps to produce the required filtering effect. Such filters are fast and simple to realize but are little stable, sensitive to temperature variations and expensive to realize in large amounts. Digital filter on the other hand uses digital processor to perform numerical calculations on sampled values of the signal and eliminate the problems associated with their classical analog counterparts, thus are preferably used in place of analog filter. Broadly, digital filters are classified as: Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filter. FIR filters have linear phase, stability, fewer finite precision errors, and efficient implementation hence preferred over IIR filter. This paper discusses the design and implementation of a FIR filter using Vedic Karastuba Multiplier and Three Adder Design. The results from the same have been obtained and observed separately. Further, the results have compared in terms of resource utilization, frequency of operation. As a result, it has been found that the Karastuba multiplier performs the same operation by reducing the number of partial products obtained at each stage thereby simplifying the architecture in terms of delay, complexity parameters.

Ms. Swetha V, Assistant Professor, Department of ECE, Dhanalakshmi Srinivasan College of Engineering and Technology, Mamallapuram, Chennai 603104 swethavijayan07@gmail.com

Mr. P.Arunkumar , Assistant Professor, Department Of ECE, Sir Issac Newton College of Engineering and Technology, Nagapattinam, 611102. kumarpece12@gmail.com

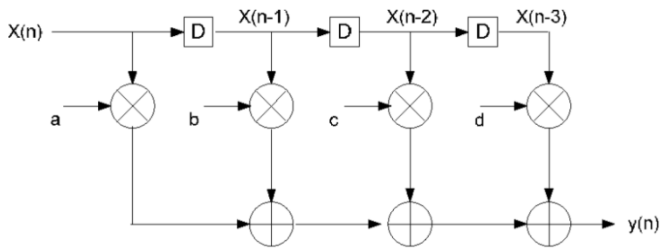
II. FINITE IMPULSE RESPONSE FILTER

A finite impulse response filter is a digital filter whose impulse response is finite in nature. The output of the FIR filter depends only on the present and the past values of the input that is it is non-recursive in nature. Hence, no feedback element is required for the filter implementation. The transfer function for the filter can be easily computed by taking the z transform of the frequency response of the FIR filter.

FIR filter transfer function can be expressed as:

$$\begin{aligned} y[n] &= b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] \\ &= \sum_{i=0}^{N} b_i \cdot x[n-i], \end{aligned}$$

x[n] is the input signal,
y[n] is the output signal,
N is the filter order;
an Nth-order filter has N+1terms on the right-hand side.



The FIR filter consists of three basic blocks: an adder block, a multiplier and some delay elements. A D flip flop can serve the purpose of delay element. The adder performs the Proposed CSLA based BEC. The Karastuba multiplier block leads to maximum delay in the design and hence needs to be optimized.

III. KARATSUBA ALGORITHM

The Karatsuba algorithm is a fast multiplication algorithm. It was discovered by Anatoly Karatsuba in 1960 and published in 1962. It reduces the multiplication of two n-digit numbers to at most single-digit multiplications in general (and exactly when n is a power of 2). Let X and Y are inputs of 'n' bits. Assuming decomposition of X and Y into 2 equal parts; XH, YH represent the higher order bits and XL, YL the lower order bits. Their product can be computed as:

$$XY = \left(2^{\frac{n}{2}}X_H + X_L\right)\left(2^{\frac{n}{2}}Y_H + Y_L\right) = 2^n(X_H Y_H) + 2^{\frac{n}{2}}(X_H Y_L + X_L Y_H) + (X_L Y_L) \quad (1)$$

In Karatsuba algorithm the computation is rewritten as:

$$X_H Y_L + X_L Y_H = (X_H + X_L)(Y_H + Y_L) - X_H Y_H - X_L Y_L \quad (2)$$

So, 4×n/2-bit multiplications can be reduced to 3×n/2-bit multiplications:

$$(X_H + Y_H)(X_L + Y_L),\ X_H Y_H \text{ and } X_L Y_L$$

Fig. 1 shows the Karatsuba multiplier at a stage when inputs are n-bits as X & Y. Output will be a Product. The steps explained by bellow Fig.

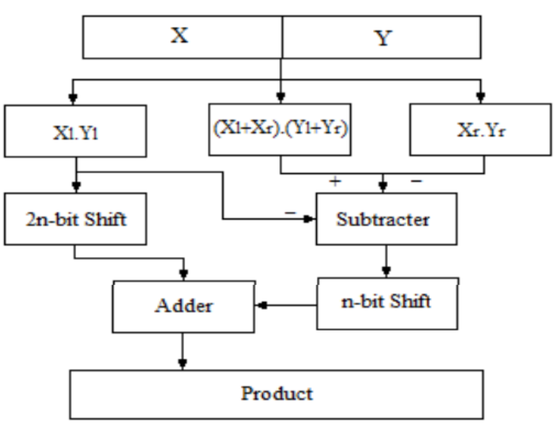
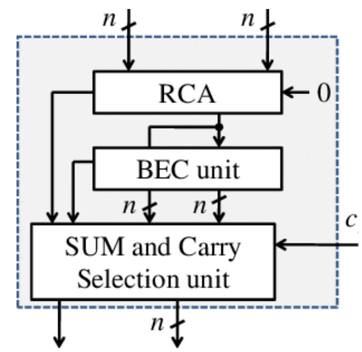


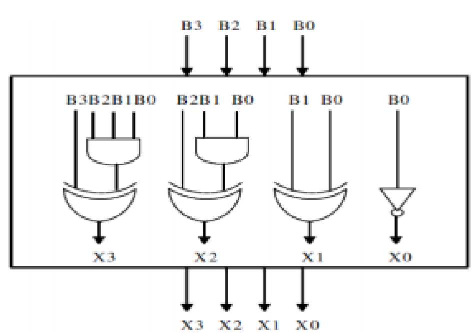
Fig1: Karatsuba Multiplier for n-Bits

IV. CARRY SELECT ADDER USING BEC

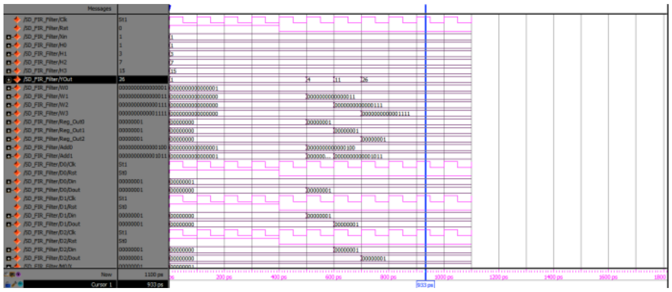
Carry Select Adder is one of the adders used in many data-processing processors to perform arithmetic functions. Carry select adder is used to increase the speed of a parallel adder that expands area in favour of speed. In 16-bit CSLA carry in is applied to 1:0 RCA and carry out is propagated to select line of mux and RCA is selected by depend upon the carry out value so if carry out is 0 then first RCA is selected and otherwise RCA is select then process is continued and increase the bit number in, RCA in every stage. 16 & 32 bit sum is obtained in this structure but area is larger because number of gate is large due to number of full adder. The structure of the 16-bit regular SQRT BEC CSLA is shown in Figure 2. The one set of 2-bit RCA in group 2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0.



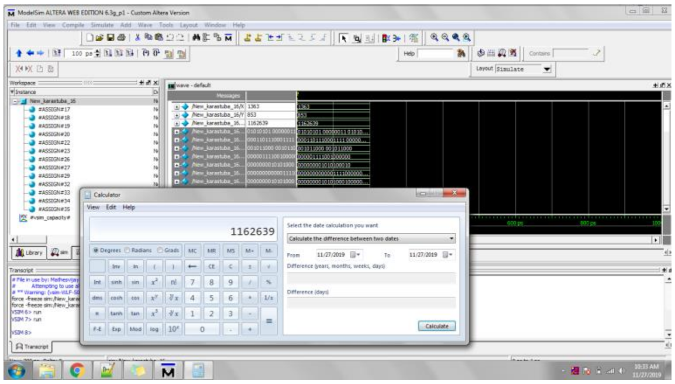
BEC is a circuit used to add 1 to the input numbers. In BEC, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus and numeral system. An N+1 bit BEC replaces the N bit RCA. BEC is instead of the RCA with reduce the area and energy consumption of the regular CSLA. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin.



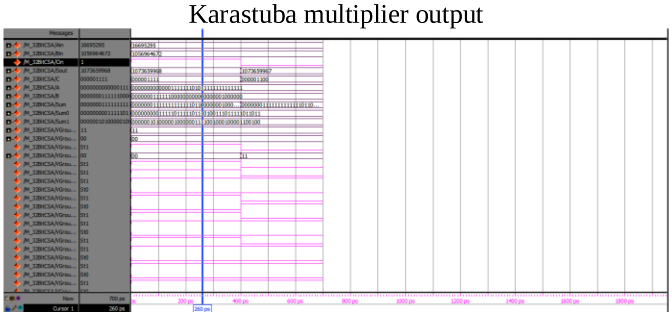
V.SIMULATION RESULTS



Fir Filter Simulation Result



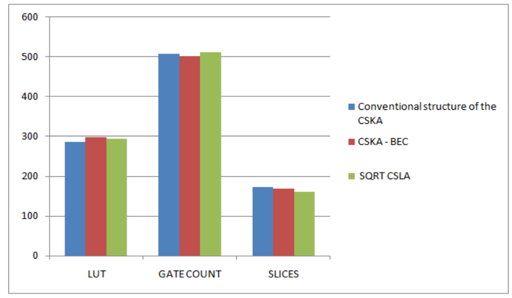
Karastuba multiplier output



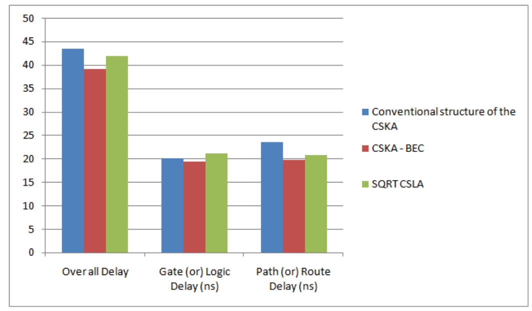
CSLA BEC Adder Output

VI. COMPARISON AND ANALYSES

METHOD NAME Design for 8x8	AREA IN NUMBER OF LUT			MEMORY IN Kilobytes	DELAY		
Device name SPARTAN 3 XC 3S 200 TQ 144	LUT	GATE COUNT	SLICES	SIZE	DELAY	GATE OR LOGIC DELAY	PATH OR ROUTE DELAY
Conventional structure of the CSKA	286	50,646	172	265052	43.452ns	20.007ns	23.445ns
CSKA - BEC	298	50,679	168	265068	39.115ns	19.453ns	19.662ns
SQRT CSLA	294	50,706	169	265064	41.862ns	21.167ns	20.695ns



Area Comparison



Delay Comparison

The Proposed FIR Filter designs are implemented using Verilog HDL, synthesized using Xilinx for different bit sizes and the delay and area have been analyzed for comparison.

From Fig. 4, it is observed that CSKA_BEC has minimum delay and it becomes lesser compared to RCA as the number of bits increases which makes it a very fast parallel adder. The results show that the use of CSKA_BEC for addition achieves overall minimum delay in the proposed multiplier at the expense of higher area and delay dissipation.

VII. CONCLUSION

Conventionally the FIR filters which have huge application in Digital Signal Processing were developed using traditional DSP algorithms. With the advancement in the technology, the FIR filters are being developed using VLSI technology. This leads to the extensive decrease in the area occupied on chip and power consumed by the filter. The FIR filter consists of three blocks: the multiplier, adder and the delay block. Out of all three, the multiplier is the slowest of all. The research work presented in this paper has achieved adequate results and has demonstrated the efficiency of high level optimization techniques. In this work, the FIR filter has been designed using Vedic karastuba and CSLA BEC Adder. From this work, it is concluded that chip area of FIR filter designed using vedic multiplier is significantly reduced and thereby making the system faster. A 16×16-bit multiplier has been proposed and designed to showcase the technique with the primary objective of minimizing the delay so that it can find application in DSP, Image Processing and computation intensive ASIPs. It is based on the Vedic Karatsuba algorithm that generates lesser number of partial product terms. The algorithm is further optimized using adaptive concept for computation of the third product term to yield faster speed.

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