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A Survey on Virtual Channel for Network-On-Chip Routers

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Abstract— This paper provides survey on virtual channel for network-on-chip routers. Virtual channel will allow only the address of the input data instead of allowing all the input bits to the output inorder to gain lower power consumption. Network-on-chip is an embedded switching network which is used to interconnect Intellectual Property (IP) cores in SOCs. NOC will improve the latency and throughput.

Keywords— Network-on-Chip(NOC), Virtual channel, power consumption, System-on-Chip(SOC), latency, throughput.

I. INTRODUCTION

The NoC technology is often called "A front-end solution to a back-end problem". As semiconductor transistor dimensions shrink and increasing amounts of IP block functions are added to a chip, the physical infrastructure that carries data on the chip and guarantees quality of service begins to crumble. Many of today's system-on-chip are too complex to utilize a traditional hierarchal bus or crossbar interconnect approach. Yesterday's village traffic has turned into today's congested freeways.To meet the growing computation-intensive applications and the needs of low-power, high-performance systems, the number of computing resources in single-chip has enormously increased, because current VLSI technology can support such an extensive integration of transistors.Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC).

Depending on four reasons SOCs need a NoCs interconnect, (i) Reduce wire routing congestion, (ii) Ease timing closure, (iii) Higher operating frequencies, (iv) Change IP easily.

II. LITERATURE SURVEY

The various approaches of virtual channel for NoC routers is described in this section

Yi Xu, Bo Zhao., [1]describes theapproach to reduce the Head-of-Line (HoL) blocking by assigning the virtual channel based on the designated output port of the packet. The approaches used for virtual channel is Fixed VC Assignment with Dynamic VC Allocation(FVADA) and Adjustable VC Assignment with Dynamic VC Allocation(AVADA). These two approaches will improve the network throughput by 41% in average and reducing the critical path delay by 60%.

NajlaAlfaraj, Junjiezhang, Yang Xu., [2] describes the hotspot congestion control for clos network on chip. Hotspot congestion control is one of the most challenging issues when designing a high throughput and low latency NoC. HOPE regulates the injected traffic rate by estimating the number of packets inside the switch network. This approach is evaluated in order to avoid the saturation tree congestion. Cost is minimal and it does not exceed 0.1% of total chip size.

MariosEvripidou, ChrysostomosNicopoulus., [3] describes virtual channel renaming by enabling the virtualization of the existing virtual channel in order to support large number of VCs. The novel concept that completely decouples the number of supported virtual channels. The virtual channel Renamer architecture will show the excellent performance without affecting the router's critical path.

ChrysostomosNicopoulus, Dongkook Park., [4] describes how virtual channels and buffer resources are allocated according to the traffic conditions in the network. The approach used for allocation is dynamic Virtual channel regulator (ViChaR). This approach will maximize the throughput by variable number of VCs on demand. The result shows the gain in performance by 25% on average. ViChaR will yield toatal area and power by 30% and 34% respectively.

MasoudOveis-Gharan, GulN.Khan., [5]describes the approach to achieve virtual channel based flow control with maximum buffer utilization. The approach discussed here is Dynamically Allocated Multi Queues(DAMQ). The linked list based methodology is used to implement DAMQ based buffers. It is also efficient to remove traffic congestion in on-chip communication for NoC systems. DAMQ will improve the latency and throughput by 30% and 23% respectively.

MasoudOveis-Gharan, GulN.Khan., [6] describes about the Index based Round Robin(IRR). In this approach all the input ports in the router functions in the index format to achieve strong fairness arbitration. It also employs a least recently served priority scheme. The architecture of IRR arbiter scales logarithmically. The behavior and architecture of IRR arbiter will leads to lower power consumption and chip area as well as higher performance characteristics.

MasoudOveis-Gharan, GulN.Khan., [7] describes the EDVC approach that is built on DAMQ buffers. The matrix arbitration method is used to get the output from the input port. The look up table is generated to hold the values which has to be executed to the output port. EDVC input port organization consumes an average power of 61% for

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application specific integrated circuits when compared to CDVC. An EDVC approach can improve NoC latency by 48-50% and throughput by 100% on average whrn compared to CDVC mechanism.

III. CONCLUSION

This paper presents a survey on different approaches for handling virtual channel for Network on Chip (NoC)routers. There are many methods to achieve the virtual channel flow control with the buffer utilization but there is still lack in this research topic. The latency, throughput, chip area, power are not measured only by using a single approach. The future work has to be enlarged as possible.

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