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A Survey on Fast Correction of Multiple Errors via Seamless Pipeline Operation

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***Abstract*—** In this paper we discuss about various testing and error correction with an example. Many Papers are taken for the survey and its advantages and disadvantages are discussed. In particular seamless pipeline operations are discussed.

***Keywords*—** Error correction, D- Latch, Low voltage operation.

I. INTRODUCTION

Testing of error is a primary concern in all sort of circuits. Setting timing guard band for the worst case is the standard way of addressing variability in circuit delay. Have to add just enough timing guardband to the critical path delay to make a circuit operate correctly in the worst case. However, the deep submicrometer nodes, process variations as well as dynamic fluctuations of supply voltage, temperature, and noise have much largerimpact on the delay. Supply voltage is continuallyscaled down with technology, since reducing operatingvoltage is the most effective way to reduce power consumption.In timing speculation the timing errors are detected and then corrected. Timing error can be detected by comparing the data from the main flip-flop with that from the shadow latch. If an error is detected, it is corrected by restoring the data from the shadow latch to the main flip-flop.This allows the timing guardband to be eliminated or to be reduced. When the timing errors occur, they are detected and corrected by on-chip circuits.

To modify the clock signal sent to the shadow latch in such a way that the shadow latch opens after the main flip-flop has captured its input data. Then the shadow latch can restore the previous, and correct, data to the main flip-flop to achieve error correction, while also capturing new input data in the same cycle. This avoids the data conflict.If any flip-flop in a stage receives a signal with critical path delay, then all the flip-flops in that stage must be replaced by RFFs.

In RFF it skip the error and have a continue process and so we unable to receive the complete signal. To overcome this i use low power flip-flop in combination of Razor flip-flop and to maintain delay period here I include D latch as buffer circuit. if error will be happen in an any received data,the entire clock will be stop because of razor based shadow latch flip-flop skip the entire portions.

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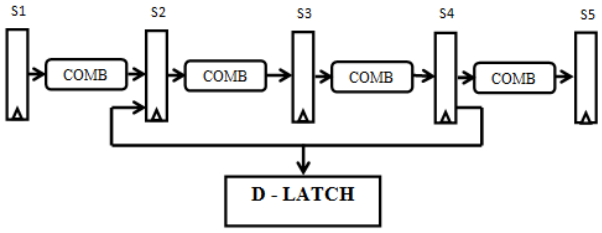

FIG 1seamless pipeline operation

In these scheme the RFFis combined with D Latch used to provide the pipeline dataThere is a combinational circuit with D latch to receive a pipeline data without any error. Error is corrected using the feed back loop of D latch.Buffer is used as a combinational circuit in this system.

Table 1
Analysis Of Testing And Error Correction

S.NO	TITLE	DESCRIPTION
1	Power minimization of pipeline architecture through 1-cycle error correction and voltage scaling	1-cycle timing error correction method enables aggressive voltage scaling in a pipelined architecture.
2	Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block	It designed using two methods ANT and RPR. ANT provides main digital signal processor and error correction. RPR corrects the error occur in output.
3	A pipeline architecture with 1-cycle timing error correction for low voltage operations	The error corrected with small scale penalty and also it avoid repeated clock gating using Razor Flip-flop
4	On Logic Synthesis On Timing Speculation	During this time, clock synthesis tools and algorithms have strove to address a myriad of important issues helping designers to create faster, more reliable, and more power efficient chips
5	Bubble Razor: Architecture Independent Timing Error Detection And Correction	Bubble Razor, an architecturally in-dependent approach to timing error detection and correction that avoids hold-time issues and enables large timing speculation windows. provides an energy efficiency improvement
6	Razor: Circuit-Level Correction Of Timing Errors For Low-Power Operation	Effective and widely used methods for power-aware computing. DVS approach that uses dynamic detection and

		correction of circuit timing errors to tune processor supply voltage and eliminate the need for voltage margins
7	TIMBER: Time Borrowing And Error Relaying For Online Timing Error Resilience	TIMBER-based error masking can recover timing margins without instruction replay or roll-back support.
8	Aging- Aware Reliable Multiplier Design With Adaptive Hold Logic	The multiplier is based on the variable-latency technique and can adjust the adaptive hold logic circuit to achieve reliable operation under the influence of Negative and Positive bias temperature instability.
9	Pulsed-latch circuits: A new dimension in ASIC design	Pulsed-latch circuits offering higher performance and lower power consumption within a conventional ASIC design environment.

II. CONCLUSION

In this paper, a low power RFF with D-latch design is presented. The proposed circuit is implemented in 90nm process. The continuous signal is passed through pipeline. The delay error is corrected in respective stages, If it continues to stage four with error then it feed back to the second stage and continues the pipeline process without error. So these methods need more area for sequential logic than counter flow pipelining.

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