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A Review On Error Correction Code

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Abstract— Error-correction codes are the codes used to correct the errors occurred during the storing of the data in the memory. The idea behind these codes is to add redundancy bits to the data being stored so that even if some errors occur due to noise in the memory, the data can be correctly stored in the memory. Bose, Ray- Chaudhuri, Hocquenghem (BCH) codes are one of the error-correcting codes. The BCH decoder consists of four blocks namely syndrome block, IBM block, chien search block and error correction block. This paper describes a new method for error detection in syndrome and chien search block of BCH decoder. The proposed syndrome block is used to reduce the number of computation by calculating the even number syndromes from the corresponding odd number syndromes. The new factorization method used to implement the algorithm of chien search block of enhanced BCH decoder reduces the number of components required. Thus, a new model of BCH decoder is proposed to reduce the area and simplify the computational scheduling of both syndrome and chien search blocks without parallelism leading to high throughput. The enhanced chase BCH decoder is designed using hardware description language called VHDL and synthesized in Xilinx ISE 14.3.

Keywords—Error correction code (ECC), static random access memory (SRAM), BCH (Bose–Chaudhuri–Hocquenghem) code.

I. INTRODUCTION

In recent years there has been an increasing demand for digital transmission and storage systems. This demand has been accelerated by the rapid development and availability of VLSI technology and digital processing. It is frequently the case that a digital system must be fully reliable, as a single error may shutdown the whole system, or cause unacceptable corruption of data, e.g. in a bank account. In situations such as this error control must be employed so that an error may be detected and afterwards corrected. The simplest way of detecting a single error is a parity checksum, which can be implemented using only exclusive-or gates. But in some applications this method is insufficient and a more sophisticated error control strategy must be implemented.

If a transmission system can transfer data in both directions, an error control strategy may be determined by detecting an error and then, if an error has occurred, retransmitting the corrupted data. These systems are called automatic repeat request (ARQ). If transmission takes place in only one direction, e.g. information recorded on a compact disk, the only way to accomplish error control is with forward error correction (FEC). In FEC systems some redundant data is concatenated with the information data in order to allow for the detection and correction of the corrupted data without having to retransmit it. One of the most important classes of FEC codes is linear block codes. In block codes, data is transmitted and corrected within one block (codeword). That is, the data preceding or following a transmitted codeword does not influence the current codeword. Linear block codes are described by the integer n, the total number of symbols in the associated codeword. Block codes are also described by the number k of information symbols within a codeword, and the number of redundant (check) symbols n-k.

As the size of embedded static random access memories (SRAMs) in a chip increases, aggressive area optimization and power optimization approaches have made them highly vulnerable to manufacturing defects and runtime failures, respectively. The vulnerability of SRAMs is even exacerbated due to the increasing process variations in nano-scale CMOS technologies. Due to process variations, SRAM cells that are marginally functional during the manufacturing test can undergo runtime failures, especially under low-voltage operation modes Error correction codes (ECCs), such as the single-error-correcting and double-error-detecting (SEC-DED) codes, are widely used to improve the reliability of on-chip SRAM memories. One of the fundamental problems encountered with the conventional uniform ECC approaches is that the ECC protection is equally applied to all memory blocks without considering the differences in importance among the data in a word of embedded memory. However, in many applications, some parts of the data in a word are much more important than other parts. For example, in the embedded memory of digital signal processor (DSP), the failures in the memory bit-cells storing high-order bits (HOBs), which are also called the most significant bits, give rise to much larger output quality degradation than those of the low-order bits (LOBs).

Considering the differences in importance in memory, modified ECC ideas have been proposed to strongly protect the HOB data bits in the embedded SRAM memories of the DSPs. Although the tradeoff between the error correction performance and area overhead is considered in the approaches, since the ECC schemes are focused on low-latency decoding, area overhead due to large parity bits and increasing decoder complexity are still very expensive. This brief presents a novel low-complexity and low-latency unequal-error-protection ECC (UEEP-ECC) for the embedded SRAM memories inside the DSPs. In the proposed ECC scheme, by efficiently merging repetition code over the Bose–Chaudhuri–Hocquenghem (BCH) code, the UEEP-ECC offers stronger error corrections on HOB parts without large area overhead due to parity bits and decoder complexity. An efficient ECC generation algorithm with low area and low-

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latency hardware architecture is also presented to achieve the minimum power consumption of memory core and ECC encoder/decoder.

II. OVERVIEW ERROR CORRECTION CODE

A. Hamming Code

In the year of 1950, Richard Hamming proposed the Hamming Codes. It is also known as Single Error Detection Codes, whichis a popular code and widely used for error control for its variation in system. This code has been considered asthe first class of linear codes for error correction. The Hamming code parameters are shown in the table1.

Table 1. Hamming code parameters

Parameters	Equations
Code length, n	n = 2^m – 1
Number of information symbols, k	k =2^m – m – 1
Number of parity-check symbols, m	n - k = m
Error-correcting capability, t	t =[(dmin - 1)/2] = 1

The first hamming code was introduced as (7,4) code. This represents that there are 4 data bits in a 7-bit packet with 3-bit parity bits, which is shown in Fig. l. For many applications, a single errorcorrecting code would be considered unsatisfactory, because itaccepts all blocks received and only capable to detect and correct a single error. However, it provides simplicity in coding and has low latency.

Bit position	D7	D6	D5	P4	D3	P2	P1
Data bit	1	0	1	1	0	1	1

Fig. 1.Hamming code (7,4)

B. Single-Error-Correction Double-Error-Detection Code

In the year of 1970, Hsiao has proposed a single error correction and double-error-detection (SEC-DED) code. This code widely used for improving computer reliability. It has been derived from the extended Hamming Code thereby itconverts from the Hamming Code by adding an extra parity bit.The SED-DED code was introduced as (8,4) code. It consisting of 4 data bits with 4extra parity bits is shown in the fig. 2. The parameters for SED-DED code are shown in the table 2.

Table.2. SED-DED parameters

Parameters	Equations
Code length, n	n = 2^m – 1
Number of information symbols	k =2^m – m – 1
Number of parity-check symbols, m	n-k =m
Error-correcting capability	dmin=3

Bit position	P8	D7	D6	D5	P4	D3	P2	P1
Data bit	1	1	0	1	1	0	1	0

Fig.2.SED-DED code (8,4)

C. Reed Solomon (RS) Code

In the year of 1960, Irving S. Reed and Gustave Solomonproposed the Reed Solomon (RS) codes. This code is a subclass of BCH codes. The RS code starts with an explanation about thetheory of Finite field (FF) or Galois Field (GF). RS code, definedwith symbols from GF(q), has the parameters are given in the table 3.

Table.3. Reed-Solomon code parameters

Parameters	Equations
Code length, n	n = q – 1
Number of parity-check symbols, m	n-k = 2m
Error-correcting capability	dmin = 2t+1

D. Low-Density Parity-Check (LDPC) Code

In the year of 1962, Robert G. Gallager proposed the LowDensityParity-Check (LDPC) codes. This LDPC codes are linear error correction code, which is defined by sparse bipartite graphs. Lowdensityparity-check codes are codes specified by a matrixcontaining mostly 0's and only a small number of 1's. Inparticular, a (n, j, k) low-density code is a code of blocklength,n with a matrix, where each column contains a smallfixed number, j, of 1 's and each row contains a small fixednumber, k, of 1's. Note that this type of matrix does not havethe check digits appearing in diagonal form.As for coding purposes, the equations can be represented asin the form of matrices to check on the sums of informationdigits. These codes are not suitable in minimizing theprobability of decoding errors like for a given block length asthe codes can only be used below the capacity of the channelwhen it is at a maximum rate. As to improve the optimality ofcodes, decoding scheme need to be simplified for low-densitycodes. Most LDPC codes have complex encoder. In

processorarchitecture, the connectivity among the decoder componentcan be large and difficult to be moved.

E. Bose-Chaudhuri-Hocquengham (BCH) Code

In year 1959, Hocquenghem initially discovered the BoseChaudhuri and Hocquenghem (BCH) codes and subsequentlyby Bose and Chaudhuri from the beginning of the year 1960. For m (m ≥3) and t(t < 2/\(m-l)), the binary BCH code parameters are shown in table 4.

Table.4.BCH code parameters

Parameters	**Equations**
Code length, n	n =2^m – 1
Number of parity-check symbols, m	n - k ≤ mt
Error-correcting capability	dmin ≥ 2t+1

The biggest advantage of BCH codes is the existence ofefficient decoding methods due to the special algebraicstructure introduced in the codes. It can detect and correct multiple errors with low latency. However, it isconsidered as a complicated code because of the complexity ofthe combinational logic circuits in the error detector.

III. CONCLUSION

In conclusion the generation of BCH codes is rather difficult and the BCS system significantly shortens the time taken to generation of BCH codes. In addition the system has been thoroughly simulated and is less error-prone than hand-crafted designs. However it should be noted that in some cases a modification of a basic BCH code is required, e.g. shortened or extended BCH codes. Furthermore a different input/output format may be required or an alarm signal needed to be asserted if an uncorrectable error pattern has occurred. BCH code can be easily adopted by changing only VHDL files that do not contain any information about finite field operators. Finally, it is worth noting that the final VHDL files are almost behavioral descriptions and that the resultant circuits are as hardware efficient as hand-crafted ones developed for just one set of parameters. Hence there are no hardware penalties incurred by using the BCS system instead of designing a BCH codes on-self, but obviously using the BCS system saves many design man hours.

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